Semester: III		
Transform, Fourier Series and Numerical Methods		
Course Code:	**MVJ21MA31D**	**CIE Marks: 50**
Credits:	**L: T:P:S: 3:2:0:0**	**SEE Marks: 50**
Hours:	**30L+20T**	**SEE Duration: 3 Hrs.**
Course Learning Objectives: The students will be able to		
1	Solve the linear differential equations using Laplace transforms	
2	Apprehend and apply Fourier transform	
3	Realize and use of Z-Transforms	
4	Use of numerical methods to solve ordinary differential equation	
5	Use of statistical methods in curve fitting applications.	

UNIT-I	
Laplace Transforms: Definition, Transforms of elementary functions, Properties, Periodic function, Unit step function. **Inverse Laplace Transforms:** Inverse Laplace Transforms, Convolution theorem to find inverse Laplace transform. Solution of linear differential equations using Laplace transforms **Self-study:** Solution of simultaneous first order differential equations. **Applications:** Analysis of electrical and electronic circuits, used in Signal processing and in control systems. **Video Link**: 1. http://nptel.ac.in/courses.php?disciplineID=111	**10 Hrs**
UNIT-II	
Fourier Transforms: Infinite Fourier transform, Infinite Fourier sine and cosine transforms, Inverse Fourier transforms, Inverse. Fourier sine and cosine transforms, Convolution theorem **Self-study:** Complex form of Fourier series. **Applications:** Fourier transforms used in image **Video Link**: 1. http://nptel.ac.in/courses.php?disciplineID=111	**10 Hrs**
UNIT-III	
Z-Transforms: Definition, standard Z-transforms, properties of Z- transforms- Shifting property, Reversal property, Multiplication by n, initial value and final value theorems. Inverse Z- transform, convolution theorem (proof and problems) Application of Z-transforms to solve difference equations. **Self-study:** Damping rule and problems on them. **Applications:** Fourier transforms used in image processing and Z-transforms in Digital	**10 Hrs**

signal processing. **Video Link**: 1. http://nptel.ac.in/courses.php?disciplineID=111	
UNIT-IV	
Numerical solution of ordinary differential equations: Numerical solution of first order and first degree; Taylor's series method, modified Euler's method, Runge-Kutta method of fourth-order. Milne's and Quadratic Spline Method. **Self-study:** Adams Bash-Method . **Applications:** To solve initial value problems **Video Link**: 1. http://nptel.ac.in/courses.php?disciplineID=111	**10 Hrs**
UNIT-V	
Statistical Methods: Correlation and regression-Karl Pearson's coefficient of correlation-problems. Regression analysis- lines of regression –problems. **Curve Fitting:** Curve fitting by the method of least squares, fitting of linear, quadratic and geometric curve. **Self-study:** A study of rank correlation. **Applications:** Applications of Correlation in Signal Processing and application of regression analysis in business **Video Link**: 1. http://nptel.ac.in/courses.php?disciplineID=111	**10 Hrs**

Course Outcomes: After completing the course, the students will be able to	
CO1	Learn to solve linear differential equations using Laplace transforms
CO2	Demonstrate Fourier Transform as a tool for solving Integral equations
CO3	Learn to evaluate Z-transform to solve difference equations.
CO4	Learn to solve algebraic, transcendental and ordinary differential equations numerically.
CO5	Make use of the correlation and regression analysis to fit a suitable mathematical model for the statistical data

Reference Books	
1.	B.S. Grewal, "Higher Engineering Mathematics" Khanna Publishers, 44th Edition, 2013.
2.	Erwin Kreyszig, "Advanced Engineering Mathematics", Wiley-India publishers, 10th edition, 2014.
3.	Prof G.B.Gururajachar "Engineering Mathematics-III , Academic Excellent series Publications, 2016-17
4.	Ramana B. V., "Higher Engineering Mathematics", Tata McGraw-Hill, 2006.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO Mapping												
CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	**3**	**3**	**0**	**3**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
CO2	**3**	**3**	**0**	**3**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
CO3	**2**	**3**	**0**	**3**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
CO4	**3**	**3**	**0**	**3**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
CO5	**3**	**3**	**0**	**2**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

Semester: III		
COMPUTER ORGANIZATION (Theory)		
Course Code: MVJ21IO32		**CIE Marks: 50**
Credits: L:T:P: 4:0:0		**SEE Marks: 50**
Hours: 50L		**SEE Duration: 3 Hrs.**

Course Learning Objectives: The students will be able to	
1	To learn the basic structure and operations of a computer.
2	To learn the arithmetic and logic unit.
3	To learn the different ways of communication with I/O devices & memories, memory hierarchies, cache memories and virtual memories.
4	To understand & implement arithmetic process.
5	To understand the processor and pipelining concepts.

UNIT-I	
Basic Structure of Computers: Basic Operational Concepts, Bus Structures, Performance –Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement. Machine Instructions and Programs: Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing, Addressing Modes, Assembly Language, Basic Input and Output Operations, Stacks and Queues, Subroutines, Additional Instructions, Encoding of Machine Instructions. Arithmetic: Numbers, Arithmetic Operations and Characters, Addition and Subtraction of Signed Numbers, Design of Fast Adders, Multiplication of Positive Numbers, Signed Operand Multiplication, Fast Multiplication, Integer Division. Laboratory Sessions/ Experimental learning: Study of peripherals, components of a Computer System Applications: Basic Computer Devices Video link: https://nptel.ac.in/courses/106105163/	**10 Hrs**
UNIT-II	

Input/output Organization: Accessing I/O Devices, Interrupts – Interrupt Hardware, Direct Memory Access, Buses, Interface Circuits. Standard I/O Interfaces – PCI Bus, SCSI Bus, USB **Laboratory Sessions/ Experimental learning**: Design of ALU **Applications**: input /output operations **Video link**: https://www.youtube.com/watch?v=RkAE4zE4uSE&list=PL13FD5F00C21BBC0B&index=11	**10 Hrs**
UNIT-III	
Memory: Basic Concepts, Semiconductor RAM Memories, Read Only Memories, Speed, Size, and Cost, Cache Memories – Types of cache, Cache miss management Mapping Functions, Replacement Algorithms, Performance Considerations, (ARM Cache and Pentium cache). **Laboratory Sessions/ Experimental learning**: Design of Memory **Applications**: Different Types of Memory **Video link**: https://nptel.ac.in/courses/106105163/	**10 Hrs**
UNIT-IV	
Processor: A Basic MIPS implementation – Building a Data path – Control Implementation Scheme –Pipelining – Pipelined data path and control – Handling Data Hazards & Control Hazards –Exceptions. **Laboratory Sessions**: Instruction scheduling **Applications**: Types of processors **Video link**: https://nptel.ac.in/courses/106106166/	**10 Hrs**
UNIT-V	
Parallelism: Parallel processing challenges –Flynn's classification – SISD, MIMD, SIMD, SPMD, and Vector Architectures - Hardware multithreading – Multi-core processors and other Shared Memory Multiprocessors - Introduction to Graphics Processing Units, Clusters, Warehouse Scale Computers and other Message-Passing Multiprocessors. **Laboratory Sessions**: Process Scheduling **Applications**: Grid and Cloud Computing **Video link**: https://nptel.ac.in/courses/106102114/	**10 Hrs**

Course Outcomes: After completing the course, the students will be able to	
CO1	Explain the basic organization of a computer system.
CO2	Demonstrate functioning of different sub systems, such as processor, Input/output, and memory.
CO3	Design and analyses simple arithmetic and logical units.
CO4	Illustrate hardwired control and micro programmed control, pipelining, embedded and other Computing systems.
CO5	Design and analyses of simple Parallelism and Multithread.

Reference Books	
3.	Carl Hamacher, Zvonko Vranesic, SafwatZaky, Computer Organization, 5th Edition, Tata McGraw Hill, 2002. (Listed topics only from Chapters 1, 2, 4, 5, and 6).
4.	David A. Patterson and John L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, Fifth Edition, Morgan Kaufmann / Elsevier, 2014.(Listed topics only from Chapters 4and 6).
3.	John P. Hayes, Computer Architecture and Organization, Third Edition, Tata McGraw Hill, 2012.
4.	John L. Hennessey and David A. Patterson, Computer Architecture – A Quantitative Approach‖, Morgan Kaufmann / Elsevier Publishers, Fifth Edition, 2012.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal

choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO Mapping												
CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	1	2	1	1	1	-	-	-	-	-	-	-
CO2	2	2	1	1	1	-	-	-	-	-	--	-
CO3	1	2	2	1	1	-	-	-	-	-	-	-
CO4	2	2	2	1	2	-	-	-	-	-	-	-
CO5	1	2	2	1	2	-	-	-	-	-	-	-

Semester: III		
OBJECT ORIENTED CONCEPTS WITH JAVA (Theory)		
Course Code: MVJ21IO33		**CIE Marks: 50**
Credits: L:T:P: 2:2:0		**SEE Marks: 50**
Hours: 40L		**SEE Duration: 3 Hrs.**

Course Learning Objectives: The students will be able to	
1	Identify the need for Java - an object-oriented language. Set up Java JDK environment to create, debug and run simple Java programs.
2	Illustrate the use of classes and distinguish the usage of different types of Inheritance and constructors in real world.
3	Demonstrate the use of exceptions and to create multi-threaded program
4	Illustrate the use of Collections with elements in Java program
5	Develop Java Application using JDBC connectivity.

UNIT-I	
Prerequisites: Basic Knowledge about C or C++ Introduction to Object Oriented Concepts and Java: Java's Magic: The Byte code; Java Development Kit (JDK); The Java Buzz words, Object Oriented Programming - Two Paradigms, Abstraction, The Three OOP Principles and its advantages, Simple Java programs. Data types, variables and arrays, Operators, Control Statements. Laboratory Sessions/ Experimental learning: A professor in college will allow a student to be excused from the final exam if either of the following is true: • They have a 90% average or higher in the class and have missed 3 or less class lectures. • They have a 80% average or higher in the class and have not missed any class lectures. The program below will determine whether a student can get out of the exam or not. Rewrite the program so only one if statement is used. Applications: Arrays in mathematical vectors, matrices. Video link / Additional online information (related to module if any): • Differences between JVM vs JRE vs JDK in Java:	**8 Hrs**

https://www.youtube.com/watch?v=5Bp6GLU6HKE	
UNIT-II	
Classes, Inheritance, Packages, and Interfaces: Classes fundamentals; Declaring objects; Assigning object reference variables; Introducing Methods, Constructors, this keyword, Finalize Method. Inheritance: Inheritance basics, using super, creating multi-level hierarchy, when constructors are called, method overriding, using abstract classes. Packages, Access Protection, Importing Packages, Interfaces. **Laboratory Sessions/ Experimental learning:** Write a program that calculates the number of buckets of paint to use for a room and the optimal number of cans to purchase. You need to ask the height of the room and the length and width of the room. The room is rectangular. You must paint the walls and the ceiling but not the floor. There are no windows or skylights. You can purchase the following size buckets of paint. • 5-liter bucket costs $15 each and covers 1500 square feet. • 1-liter bucket costs $4 and covers 300 square feet. **Applications:** Inheritance in Banking Sectors **Video link / Additional online information (related to module if any):** Types of Inheritance: https://www.youtube.com/watch?v=ZP27c7i5zpg	**8 Hrs**
UNIT-III	
Exception Handling and Multi-Threaded Programming: Exception Handling fundamentals, Exception Types, Uncaught Exceptions, Using try catch, Multiple catch clauses, Nested try statements, throw, throws, finally, Java's built-in exceptions, Programming Examples. **Multi-Threaded Programming**: The java thread model, Main thread, Creating Thread, creating multiple threads, Using is Alive () and join (), Thread priorities, Synchronization; Inter Thread Communication - Bounded buffer problem. **Laboratory Sessions/ Experimental learning:**	**8 Hrs**

The Producer-Consumer problem describes two processes, the producer, and the consumer, which share a common, fixed-size buffer used as a queue. The producer's job is to generate data, put it into the buffer, and start again. At the same time, the consumer is consuming the data (i.e., removing it from the buffer), one piece at a time. Make sure that the producer won't try to add data into the buffer if it's full and that the consumer won't try to remove data from an empty buffer. Write a java code to get the solution for this multi-process synchronization problem. **Applications:** Multithreads in Browsers, Servers **Video link / Additional online information (related to module if any):** Multithreading: https:/youtu.be/QFbxzynUij4	
UNIT-IV	
The collections and Framework: Collections Overview, Recent Changes to Collections, The Collection Interfaces, The Collection Classes, accessing a collection Via an Iterator, Storing User Defined Classes in Collections. **Java Lambda expressions:** Java Lambda expressions, Using Java Lambda expressions, Lambda expression vs method in java, Lambda expression in the array list. **Laboratory Sessions/ Experimental learning:** Write a Java program to iterate through all elements in a array list. Write a Java program to create a new array list, add some colours (string) and print out the collection **Applications:** Elements in group **Video link / Additional online information (related to module if any):** https://www.youtube.com/watch?v=Q_9vV3H-dt4	**8 Hrs**
UNIT-V	
JDBC: The Concept of JDBC; JDBC Driver Types; JDBC Packages; A Brief Overview of the JDBC process; Database Connection; Associating the	**8 Hrs**

JDBC/ODBC Bridge with the Database; Statement Objects; Result Set; Transaction Processing; Metadata, Data types; Exceptions. **Laboratory Sessions/ Experimental learning:** Develop Student Management System application with swings as the front end and database as the back end using JDBC connectivity. **Applications**: Scientific Applications, Financial Applications **Video link / Additional online information (related to module if any):** Java JDBC: https://www.youtube.com/watch?v=hEWBIJxrLBQ	

Course Outcomes: After completing the course, the students will be able to	
CO1	Illustrate the Object-Oriented Programming concepts and basic characteristics of Java.
CO2	Demonstrate the principles of classes, inheritance, packages and interfaces.
CO3	Experiment with exception handling Mechanisms and Create multi-threaded programs.
CO4	Interpret the need for advanced Java concepts like collections in developing modular and efficient programs.
CO5	Develop an application with Database using JDBC connectivity.

Reference Books	
1.	Herbert Schildt, "Java The Complete Reference", 7 /9th Edition, Tata McGraw Hill, 2007.
2.	Jim Keogh: "J2EE-The Complete Reference", McGraw Hill, 2007.
3.	"Effective Java", Third Edition, Joshua Bloch, Addison-Wesley Professional,2017
4.	Richard Warburton, Java 8 Lambdas: "Pragmatic Functional Programming" Kindle Edition.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO Mapping												
CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	**1**											
CO2	**1**		**2**	**2**			**1**			**2**	**2**	
CO3	**1**							**2**	**2**	**2**	**1**	
CO4	**1**	**2**				**2**						**2**
CO5	**1**	**2**				**2**						**2**

Semester: III		
INTRODUCTION TO EMBEDDED SYSTEM DESIGN (Theory and Practice)		
Course Code: MVJ21IO34		**CIE Marks:50+50**
Credits: L:T:P: 3:0:1		**SEE Marks: 50 +50**
Hours:40 L+ 26 P		**SEE Duration: 03+03 Hours**

Course Learning Objectives: The students will be able to	
1	Explain the fundamentals of ARM based system, basic hardware components, selection methods and attributes of an ARM Controller.
2	Program ARM controller using the various instructions.
3	Explain the fundamentals of Exception, Interrupt Handling and Memory Management Unit of ARM Controller.
4	Identify the Embedded System Design applications.
5	Explain the real time operating system for the embedded system design.

UNIT-I	
ARM EMBEDDED SYSTEMS: *Prerequisites:* ARM DESIGN PHILOSOPHY, ARM DATAFLOW MODEL Microprocessors versus Microcontrollers, ARM Embedded Systems: The RISC design philosophy, The ARM Design Philosophy, Embedded System Hardware, Embedded System Software. ARM Processor Fundamentals: Registers, Current Program Status Register, Pipeline, Exceptions, Interrupts, and the Vector Table, Core Extensions Laboratory Sessions/ Experimental learning: 1.Comparision of Microprocessor and Microcontroller hardware Model 2.Comparing the Microprocessor and Microcontroller Software Model Applications: Smartphones, Tablets, Wearables Video link / Additional online information: 1. https://www.youtube.com/watch?v=DMsL6TVS0IQ https://www.youtube.com/watch?v=JPfG0UQd3x4	**10 Hrs**
UNIT-II	
ARM Instruction Set and Programming	**10 Hrs**

Prerequisites: ARM INSTRUCTION SET,ARM ASSEMBLY PROGRAMMING **Introduction to the ARM Instruction Set** : Data Processing Instructions , Programme Instructions, Software Interrupt Instructions, Program Status Register Instructions, Coprocessor Instructions, Loading Constants **ARM programming using Assembly language**: Writing Assembly code, Profiling and cycle counting, instruction scheduling Laboratory Sessions/ Experimental learning: 1.Writing ARM Assembly program for Embedded System Applications **Applications**: Coding Device Drivers, Real-Time Systems, Low-Level Embedded Systems, Boot Codes, Reverse Engineering **Video link / Additional online information:** https://www.youtube.com/watch?v=gfmRrPjnEw4	
UNIT-III	
Interrupt and Memory Management Unit: *Prerequisites:* Interrupt, Exception, Memory Management unit **Exception, Interrupt Handling** : Exception handling, Interrupts, Interrupt handling Schemes **Memory Management Unit** : The Memory Hierarchy and Cache Memory, Cache Architecture, Cache Policy, Moving from MPU to an MMU, How Virtual Memory Works, Details of ARM MMU Laboratory Sessions/ Experimental learning: 1) Use of External interrupt0 to turn ON/OFF led connected to Pin P1.25 of ARM Processor. 2) Use of Software Interrupt SWI instruction in programming. 3) Calculating physical memory address from logical address.	**10 Hrs**

Applications: Internal Errors and Special Conditions Management, Hardware Concurrency, and Service Requests Management. Video link / Additional online information: 1. https://www.youtube.com/watch?v=-Dt9EDsMHiI https://www.youtube.com/watch?v=Kju5UMLC7hg	
UNIT-IV	
Prerequisites: Embedded systems, Embedded Applications **Embedded System Components:** Embedded Vs General computing system, History of embedded systems, Classification of Embedded systems, Major applications areas of embedded systems, purpose of embedded systems Core of an Embedded System including all types of processor/controller, Memory, Sensors, Actuators, LED, 7 segment LED display, stepper motor, Keyboard, Push button switch, Communication Interface (on board and external types), Embedded firmware, Other system components. **Laboratory Sessions/ Experimental learning:** Digital Clock, Battery operated Smartcard Reader **Applications:** Home Appliances, Office Automation, Security, Telecommunication **Video link / Additional online information:** 1. https://www.youtube.com/watch?v=SD65b5cYfdI https://www.youtube.com/watch?v=obknO3gA92E	**10 Hrs**
UNIT-V	
Prerequisites: Real time operating system **Real Time Operating System (RTOS) based Embedded System Design:** Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread pre-emption, Multiprocessing and Multitasking, Task Communication (without any program), Task synchronization issues – Racing and	**10 Hrs**

Deadlock, Concept of Binary and counting semaphores (Mutex example without any program), How to choose an RTOS Laboratory Sessions/ Experimental learning: Automated Meter Reading System (AMR) and Digital Camera, Real time concepts Applications: Industrial Control, Telephone Switching Equipment, Flight Control, and Real-Time Simulations Video link / Additional online information: https://www.youtube.com/watch?v=T54qJMqpim8	

LABORATORY EXPERIMENTS

1. Write a program to find the sum of first 10 integer numbers.
2. Write a program to find factorial of a number.
3. Write a program to add an array of 16 bit numbers and store the 32 bit result in internal RAM
4. Write a program to find the square of a number (1 to 10) using look-up table.
5. Write a program to find the largest/smallest number in an array of 32 numbers
6. Write a program to arrange a series of 32 bit numbers in ascending/descending order
7. Write a program to count the number of ones and zeros in two consecutive memory locations
8. Write an ARM assembly program that checks if a 32-bit number is a palindrome. Assume that the input is available in r 3. The program should set r 4 to 1 if it is a palindrome, otherwise r 4 should have 0. A palindrome is a number which is the same when read from both sides. For example, 1001 is a 4 bit palindrome.
9. Display "Hello World" message using Internal UART
10. Interface and Control a DC Motor
11. Interface a Stepper motor and rotate it in clockwise and anti-clockwise direction
12. Interface a DAC and generate Triangular and Square waveforms.
13. Display the Hex digits 0 to F on a 7-segment LED interface, with an appropriate delay in Between

STUDY EXPERIMENT

1. Interface a 4x4 keyboard and display the key code on an LCD

Any 12 experiments to be conducted

Course Outcomes: After completing the course, the students will be able to	
CO1	Describe the architectural features and instructions of ARM microcontroller

CO2	Develop Assembly Programs in ARM for Embedded applications.
CO3	Describe the fundamentals of Exception, Interrupt Handling and Memory Management Unit of ARM Controller
CO4	Interface external devices and I/O with ARM microcontroller.
CO5	Demonstrate the need of real time operating system for embedded system applications

Reference Books	
1.	Andrew N Sloss, Dominic Symes and Chris Wright, ARM system developer's guide, Elsevier, Morgan Kaufman publishers, 2008.
2.	Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education, Private Limited, 2nd Edition.
3.	Raghunandan.G.H, "Microcontroller (ARM) and Embedded System", Cengage learning Publication, 2019
4.	"The Insider's Guide to the ARM7 Based Microcontrollers", Hitex Ltd., 1st edition, 2005.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Laboratory- 50 Marks

The laboratory session is held every week as per the time table and the performance of the student is evaluated in every session. The average of the marks over number of weeks is considered for 30 marks. At the end of the semester a test is conducted for 10 marks. The students are encouraged to implement additional innovative experiments in the lab and are awarded 10 marks. Total marks for the laboratory is 50.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks are executed by means of an examination.

The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three

sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of Cos and Bloom's taxonomy level.

CO-PO/PSO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	1	2	1	-	-	-	-	-	-	-	-
CO2	3	2	1	3	3	2	-	-	2	-	1	-
CO3	3	2	1	3	-	2	-	-	2	-	-	-
CO4	3	3	2	3	3	2	-	-	2	2	2	-
CO5	3	2	3	3	3	2	-	-	2	2	2	2

Semester: III		
ANALOG AND DIGITAL ELECTRONICS (Theory and Practice)		
Course Code: MVJ21IO35		**CIE Marks:50+50**
Credits: L:T:P: 3:0:1		**SEE Marks: 50 +50**
Hours:40 L+ 26 P		**SEE Duration: 03+03 Hours**
Course Learning Objectives: The students will be able to		
1	Explain the use of photo electronics devices, 555 timer IC, Regulator ICs and uA741.	
2	Make use of simplifying techniques in the design of combinational circuits.	
3	Illustrate combinational and sequential digital circuits.	
4	Demonstrate the use of flipflops and apply for registers.	
5	Design and test counters, Analog-to-Digital and Digital-to-Analog conversion techniques.	

UNIT-I	
Prerequisites: BJT Transistor BJT Biasing: Fixed bias, Collector to base Bias, voltage divider bias Operational Amplifier Application Circuits: Peak Detector, Schmitt trigger, Active Filters, Non-Linear Amplifier, Relaxation Oscillator, Current-to-Voltage and Voltage-to-Current Converter, Regulated Power Supply Parameters, adjustable voltage regulator, D to A and A to D converter. Laboratory Sessions/ Experimental learning: 1. Simulate BJT CE voltage divider biased voltage amplifier using any suitable circuit simulator. 2. Design an astable multivibrator circuit for three cases of duty cycle (50%, <50% and >50%) using NE 555 timer IC. 3. Using ua 741 opamap, design a window comparator for any given UTP and LTP. Applications: Design a integrated power supply and function generator operating at audio frequency. Sine, square and triangular functions are to be generated.	**10 Hrs**

Video link / Additional online information: 1. https://www.youtube.com/watch?v=l6M6FvjUdTI https://www.youtube.com/watch?v=kiiA6WTCQn0&list=PLwjK_iyK4LLDBB1E9MFbxGCEnmMMOAXOH	
UNIT-II	
Karnaugh maps: minimum forms of switching functions, two and three variable Karnaugh maps, four variable Karnaugh maps, determination of minimum expressions using essential prime implicants **Quine-McClusky Method:** determination of prime implicants, the prime implicant chart, Petricks method, simplification of incompletely specified functions, simplification using map-entered variables Laboratory Sessions/ Experimental learning: 1. Given a 4-variable logic expression, simplify it using appropriate technique and inplement the same using basic gates. **Applications:** Logic gates simplification Video link / Additional online information: 1. https://www.youtube.com/watch?v=BPBiyzc0OBw https://www.youtube.com/watch?v=QIs7YbV6htg	**10 Hrs**
UNIT-III	
Combinational circuit design and simulation using gates: Review of Combinational circuit design, Full Adder & Subtractors, Parallel Adder and Subtractor, Look ahead carry Adder, Binary comparators, Hazards in combinational Logic, simulation and testing of logic circuits **Multiplexers, Decoders and Programmable Logic Devices:** Multiplexers, Multiplexers & Demultiplexer, Decoders & Multiplexers as minterm /maxterm Generator, Decoder, Encoders, Programmable Logic devices. Laboratory Sessions/ Experimental learning: 1. Design a full adder using two half adders in Pspice tool. 2. Design an Adder cum Subtractor circuit which adds when input bit operation=1 or subtract if 0, using Pspice. 3. Realize a Boolean expression using decoder IC74139.	**10 Hrs**

4. Design and implement code converter I) Binary to Gray (II) Gray to Binary Code **Applications:** Audio and Video transmission. **Video link / Additional online information:** 1. https://www.youtube.com/watch?v=RZQTTfU9TNA, 2. https://www.youtube.com/watch?v=36hCizOk4PA, 3. https://www.youtube.com/watch?v=397DDnkBm8A&t=42s	
UNIT-IV	
Sequential Circuit Design: Characteristic equations, Asynchronous Counter, Design of a synchronous mod-n counter using clocked JK, D, T and SR flip-flops, Mealy& Moore Models, Synchronous Sequential circuit Analysis. **HDL Concepts**: Sequential circuit design on Synchronous and Asynchronous Counters in Verilog. **Laboratory Sessions/ Experimental learning:** 1. Design a Synchronous Counter for a given sequence- 0, 2, 4, 6, 0 using Verilog. 2. Design a 4-bit Asynchronous up/down counter using Pspice tool (D, T, JK, SR flipflops) 3. Design a 4-bit binary Synchronous up/down counter using Pspice tool. (D, T, JK, SR flipflops) 4. Design Pseudo Random Sequence generator using 7495 **Applications:** Data synchronizer, Counter. **Video link / Additional online information:** 1. https://www.youtube.com/watch?v=O3If0Nr9to0	**10 Hrs**
UNIT-V	
Registers and Counters: Registers and Register Transfers, Parallel Adder with accumulator, shift registers, design of Binary counters, counters for other sequences, counter design using SR and J K Flip Flops. **Synthesis Basics**: Introduction, Synthesis information from Entity and Module, Mapping Process and Always in the Hardware Domain. Laboratory Sessions/ Experimental learning:	**10 Hrs**

1. Design and implement a mod-n (n<8) synchronous up counter using J-K Flip-Flop ICs and demonstrate its working.

2. Design and implement an asynchronous counter using decade counter IC to count up from 0 to n (n<=9) and demonstrate on 7-segment display (using IC-7447)

Applications: Timing verification, test documentation.

Video link / Additional online information:

https://nptel.ac.in/courses/117108040/

LABORATORY EXPERIMENTS

1. Design Adder, Integrator and Differentiator using Op-Amp.
2. Design instrumentation amplifier of a differential mode gain of "A" using three Amplifiers.
3. Verify
   (a) Demorgan's Theorem for 2 variables.
   (b) The sum-of product and product-of-sum expressions using universal gates.
4. Design and implement
   (a) Full Adder using basic logic gates.
   (b) Full subtractor using basic logic gates.
5. (a)Design and implement (i) 4-bitParallelAdder/ Subtractor using IC 7483. (ii) BCD to Excess-3 code conversion and vice-versa.

   (b)Realize (i) Adder & Subtractors using IC 74153(ii) 4-variable function using IC 74151(8:1MUX)
6. Realize the following flip-flops using NAND Gates.(a) Clocked SR Flip-Flop (b) JK Flip-Flop (c) D-Flip-Flop
7. Realize the following shift registers using IC7474
   a.SISO (b) SIPO (c) PISO (d) PIPO (e) Ring Counter (f) Johnson Counter.
8. Realize (i) Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop (ii) Mod-N Counter using IC7490 / 7476.
9. Write a Verilog program for the following combinational designs a) 2 to 4 decoder b) 8 to 3 (encoder without priority & with priority) c). 8 to 1 multiplexer d) 4 bit binary to gray converter e) Multiplexer, De-multiplexer, Comparator.
10. Design 4 bit binary, BCD counters with Synchronous reset and asynchronous reset and "any sequence"counters using Verilog code.
11. Write HDL code to display messages on alpha numeric LCD display.
12. Write a HDL code to accept Analog signal, Temperature sensor and display the data on LCD or Seven Segment Display.

Any 12 experiments to be conducted

Course Outcomes: After completing the course, the students will be able to	
CO1	Design and analyze application of analog circuits using photo devices, timer IC, power supply and regulator IC and op-amp.
CO2	Illustrate simplification of Algebraic equations using K-map & Quine-McCluskey Technique.
CO3	Analyze & design different applications of Combinational & Sequential Circuits to meet desired need within realistic constraints.
CO4	Write code & verify the functionality of digital circuit/system using test benches to solve engineering problems in digital circuits.
CO5	Know the importance of Synthesis & counters used for designing digital circuits.

Reference Books	
1.	Charles H Roth and Larry L Kinney and Raghunandan G H Analog and Dig Electronics, Cengage Learning,2019
2.	John M Yarbrough, "Digital Logic Applications and Design", Thomson Learning, 2001.
3.	Donald D. Givone, "Digital Principles and Design", McGraw Hill, 2002.
4.	Samir Palnitkar "Verilog HDL: A Guide to Digital Design and Synthesis", Pearson Education, Second Edition

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Laboratory- 50 Marks

The laboratory session is held every week as per the time table and the performance of the student is evaluated in every session. The average of the marks over number of weeks is considered for 30 marks. At the end of the semester a test is conducted for 10 marks. The students are encouraged to implement additional innovative experiments in the lab and are awarded 10 marks. Total marks for the laboratory is 50.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks are executed by means of an examination.

The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	1	1	1	-	-	-	-	-	-	-
CO2	1	-	-	-	3	-	-	-	-	-	-	-
CO3	1	2	3	-	3	-	-	-	-	-	-	-
CO4	1	2	2	2	3	-	-	-	-	-	-	-
CO5	1	1	1	-	2	-	-	-	-	-	-	-

Course Title	CONSTITUTION OF INDIA, PROFESSIONAL ETHICS AND CYBER LAW	Semester	III/IV
Course Code	MVJ21IO36	CIE	50
Total No. of Contact Hours	15	SEE	50
No. of Contact Hours/week	1 (L : T : P :: 1 :0 : 0)	Total	100
Credits	1	Exam. Duration	1 Hour

Course objective is to:

- To know the fundamental political codes, structure, procedures, powers, and duties of Indian constitution, Indian government institutions, fundamental rights, directive principles and the duties of the citizens.

• To provide overall legal literacy to the young technocrats to manage complex societal issues in the present scenario. • To understand engineering ethics & their responsibilities, identify their individual roles and ethical responsibilities towards society.		
Module-1	RBT Level L1,L2,L3	3Hrs.
Introduction to Indian Constitution: The Necessity of the Constitution, The Societies before and after the Constitution adoption. Introduction to the Indian Constitution, The Making of the Constitution, The role of the Constituent Assembly – Preamble and Salient features of the Constitution of India. Fundamental Rights and its Restriction and Limitations in different Complex Situations. Directive Principles of State Policy (DPSP) and its present relevance in our society with examples. Fundamental Duties and its Scope and Significance in Nation Building.		
Module – II	RBT Level L1,L2,L3	3Hrs.
Union Executive and State Executive: Parliamentary System, Federal System, Centre-State Relations. Union Executive – President, Prime Minister, Union Cabinet, Parliament - LS and RS, Parliamentary Committees, Important Parliamentary Terminologies. Supreme Court of India, Judicial Reviews and Judicial Activism. State Executives – Governor, Chief Minister, State Cabinet, State Legislature, High Court and Subordinate Courts, Special Provisions (Article 370, 371, 371J) for some States.		
Module – III	RBT Level L1,L2,L3	3Hrs.
Elections, Amendments and Emergency Provisions: Elections, Electoral Process, and Election Commission of India, Election Laws. Amendments - Methods in Constitutional Amendments (How and Why) and Important Constitutional Amendments. Amendments – 7,9,10,12,42,44,61,73,74,75,86, and 91,94,95,100,101,118 and some important Case Studies. Recent Amendments with explanation. Important Judgements with Explanation and its impact on society (from the list of Supreme		

Court Judgements). Emergency Provisions, types of Emergencies and its consequences. **Constitutional Special Provisions:** Special Constitutional Provisions for SC & ST, OBC, Special Provision for Women, Children & Backward Classes.		
Module – IV	**RBT Level L1,L2,L3**	3Hrs.
Professional / Engineering Ethics: Scope & Aims of Engineering & Professional Ethics - Business Ethics, Corporate Ethics, Personal Ethics. Engineering and Professionalism, Positive and Negative Faces of Engineering Ethics, Code of Ethics as defined in the website of Institution of Engineers (India): Profession, Professionalism, Professional Responsibility. Clash of Ethics, Conflicts of Interest. **Responsibilities in Engineering** - Responsibilities in Engineering and Engineering Standards, the impediments to Responsibility. Trust and Reliability in Engineering, IPRs (Intellectual Property Rights), Risks, Safety and liability in Engineering.		
Module – V	**RBT Level L1,L2,L3**	3Hrs.
Internet Laws, Cyber Crimes and Cyber Laws: Internet and Need for Cyber Laws, Modes of Regulation of Internet, Types of cyber terror capability, Net neutrality, Types of Cyber Crimes, India and cyber law, Cyber Crimes and the information Technology Act 2000, Internet Censorship, Cybercrimes and enforcement agencies.		

Course Outcomes: On completion of this course, students will be able to	
CO1	Have constitutional knowledge and legal literacy
CO2	Understand Engineering and Professional ethics and responsibilities of Engineers.
CO3	Understand the cybercrimes and cyber laws for cyber safety measure.

Text Books:

1.	Constitution of India and Professional Ethics, T.S. Anupama, Sunstar Publisher
Reference Books:	
1.	Durga Das Basu (DD Basu): "Introduction to the Constitution on India", (Students Edition.) Prentice –Hall EEE, 19th/20th Edn., (Latest Edition) or 2008.
2.	Shubham Singles, Charles E. Haries, and Et al : "Constitution of India and Professional Ethics" by Cengage Learning India Private Limited, Latest Edition – 2018.
3	M.Govindarajan, S.Natarajan, V.S.Senthilkumar, "Engineering Ethics", Prentice – Hall of India Pvt. Ltd. New Delhi, 2004.
4.	M.V.Pylee, "An Introduction to Constitution of India", Vikas Publishing, 2002.
5.	Latest Publications of NHRC - Indian Institute of Human Rights, New Delhi.

Semester: III		
Additional Mathematics-I **(Common to all branches)**		
Course Code:	**MVJ21MATDIP1**	**CIE Marks:50**
Credits:	**L:T:P:S: 4:0:0:0**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	To familiarize the important and introductory concepts of Differential calculus	
2	Aims to provide essential concepts integral calculus	
3	To gain knowledge of vector differentiation	
4	To learn basic study of probability	
5	Ordinary differential equations of first order and analyze the engineering problems.	

UNIT-I	
Differential calculus: Recapitulation of successive differentiation -nth derivative -Leibnitz theorem (without proof) and Problems, Polar curves - angle between the radius vector and tangent, angle between two curves, pedal equation, Taylor's and Maclaurin's series expansions- Illustrative examples. **Video Link**: 1. http://nptel.ac.in/courses.php?disciplineID=111	**8 Hrs**
UNIT-II	
Integral Calculus: Statement of reduction formulae for the integrals of $\sin^n(x)$, $\cos^n(x)$, $\sin^n(x)\cos^n(n)$ and evaluation of these integrals with standard limits-problems. Double and triple integrals-Simple examples. **Video Link**: 1. http://nptel.ac.in/courses.php?disciplineID=111	**8 Hrs**
UNIT-III	
Vector Differentiation: Scalar and Vector point functions, Gradient, Divergence, Curl, Solenoidal and Irrotational vector fields. **Vector identities** - $div(\phi\vec{A}), curl(\phi\vec{A}), curl(grad(\phi)), div(curl\ \vec{A})$. **Video Link**: 1. http://nptel.ac.in/courses.php?disciplineID=111	**8Hrs**
UNIT-IV	
Probability: Basic terminology, Sample space and events. Axioms of probability. Conditional probability – illustrative examples. Bayes theorem-examples. **Video Link**: 1. http://nptel.ac.in/courses.php?disciplineID=111	**8Hrs**
UNIT-V	
Ordinary Differential Equations of First Order: Introduction – Formation of differential equation, solutions of first order and first degree differential equations: variable separable form, homogeneous, exact, linear differential equations. **Video Link**: 1. http://nptel.ac.in/courses.php?disciplineID=111	**8Hrs**

Course Outcomes: After completing the course, the students will be able to	
CO1	Apply the knowledge of calculus to solve problems related to polar curves and its applications
CO2	Apply the concept of integration and variables to evaluate multiple integrals and their usage in computing the area and volumes.
CO3	Illustrate the applications of multivariate calculus to understand the solenoidal and irrotational vectors and also exhibit the inter dependence of line, surface and volume integrals.
CO4	Understand the basic Concepts of Probability
CO5	Recognize and solve first-order ordinary differential equations occurring in different branches of engineering.

Reference Books	
1.	B.S. Grewal, Higher Engineering Mathematics**,** Khanna Publishers, 43rd Edition**,** 2013**,** .
2.	G. B. Gururajachar, Calculus and Linear Algebra, Academic Excellent Series Publication, 2018-19
3.	Chandrashekar K. S, Engineering Mathematics-I, Sudha Publications, 2010.

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Theory for 50 Marks

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Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

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CO1	3	3	0	2	0	0	0	0	0	0	1	1

CO2	3	3	0	2	0	0	0	0	0	0	1	1
CO3	3	3	0	3	0	0	0	0	0	0	1	1
CO4	2	2	0	3	0	0	0	0	0	0	1	1
CO5	2	2	0	2	0	0	0	0	0	0	0	1