Course Title	Discrete Math & Probability Theory	**Semester**	III
Course Code	MVJ19MIS31	**CIE**	50
Total No. of Contact Hours	60 L : T : P :: 40 : 0 : 20	**SEE**	50
No. of Contact Hours/week	3	**Total**	100
Credits	3	**Exam. Duration**	3 Hours

Course objective is to:

- Prepare for a background in abstraction, notation, and critical thinking for the mathematics most directly related to computer science.
- Understand and apply mathematical induction, combinatorics, discrete probability, sequence and recurrence, elementary number theory.
- Understand and apply probability distribution, sampling theory and joint probability distributions.

Module-1	**L1,L2,L3**	**12 Hours**

Properties of the Integers: The Well Ordering Principle – Mathematical Induction.

Principles of Counting: Fundamental Principles of Counting, The Rules of Sum and Product, Permutations, Combinations – The Binomial and Multinomial Theorem, Combinations with Repetition.

Application: Distribution with repetition.

Video Link:
1. http://nptel.ac.in/courses.php?disciplineID=111
2. http://www.class-central.com/subject/math(MOOCs)
3. http://academicearth.org/

Module-2	**L1,L2,L3**	**12 Hours**

The Principle of Inclusion and Exclusion: The Principle of Inclusion and Exclusion, Generalizations of the Principle. Derangements – Nothing is in its Right Place, Rook Polynomials.

Recurrence Relations: First Order Linear Recurrence Relation, The Second Order Linear Homogeneous Recurrence Relation with Constant Coefficients.

Application: Arrangement with forbidden position.

Video Link:
1. http://nptel.ac.in/courses.php?disciplineID=111
2. http://www.class-central.com/subject/math(MOOCs)
3. http://academicearth.org/

Module-3	**L1,L2,L3**	**12 Hours**

Relations: Cartesian Products, Relations, Properties of Relations, Computer Recognition – Zero-One Matrices and Directed Graphs, Partial Orders – Hasse Diagrams, Equivalence Relations and Partitions. Functions: Plain and One to One, Onto Functions. The Pigeon-hole Principle, Function Composition and Inverse Functions.

Application: Zero-one matrix and Hasse diagram

Video Link:
1. http://nptel.ac.in/courses.php?disciplineID=111
2. http://www.class-central.com/subject/math(MOOCs)
3. http://academicearth.org/

Module-4	**L1,L2,L3**	**12 Hours**

Probability Distributions: Random variables (discrete and continuous), probability mass/density functions. Binomial distribution, Poisson distribution. Exponential and normal distributions, problems. Joint probability distribution: Joint Probability distribution for two discrete random variables, expectation, covariance, correlation coefficient.

Application: Finding correlation between random variables.

Video Link:
1. http://nptel.ac.in/courses.php?disciplineID=111
2. http://www.class-central.com/subject/math(MOOCs)
3. http://academicearth.org/

Module-5	**L1,L2,L3**	**12 Hours**

Sampling Theory: Sampling, Sampling distributions, standard error, test of hypothesis for means and proportions, confidence limits for means, student's t-distribution and Chi-square distribution.

Coding Theory: Coding of binary information and error detection, decoding and error detection.

Application: Testing the level of significance & the goodness of fit for large sample and small sample.

Video Link:
1. http://nptel.ac.in/courses.php?disciplineID=111
2. http://www.class-central.com/subject/math(MOOCs)
3. http://academicearth.org/

Course outcomes:

CO1	Demonstrate the application of discrete structures in different fields of computer Science.
CO2	Solve problems using recurrence relations and generating functions.
CO3	Solving logical problem using concepts of relations and functions.
CO4	Develop probability distribution of discrete, continuous random variables and joint probability distribution occurring in digital signal processing, information theory and Design engineering.
CO5	Demonstrate testing of hypothesis of sampling distributions.

Reference Books:

1.	Ralph P. Grimaldi: Discrete and Combinatorial Mathematics, 5th Edition, Pearson Educatio 2004.
2.	B.S. Grewal, "Higher Engineering Mathematics" Khanna Publishers, 43rd Edition, 2013.
3.	Ramana B. V., "Higher Engineering Mathematics", Tata Mc Graw-Hill, 2006.
4.	Kenneth H. Rosen: Discrete Mathematics and its Applications, 6th Edition,

	McGraw Hill, 2007
5.	Basavaraj S Anami and Venakanna S Madalli: Discrete Mathematics – A Concept based approach, Universities Press, 2016.

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	0	3	0	0	0	0	0	0	1	1
CO2	2	3	0	3	0	0	0	0	0	0	1	1
CO3	2	3	0	3	0	0	0	0	0	0	1	1
CO4	3	3	0	3	0	0	0	0	0	0	1	1
CO5	3	3	0	3	0	0	0	0	0	0	1	1

High-3, Medium-2, Low-1

Course Title	Data Structure	**Semester**	III
Course Code	MVJ19IS32	**CIE**	50
Total No. of Contact Hours	60 L : T : P :: 40 : 0 : 20	**SEE**	50
No. of Contact Hours/week	4	**Total**	100
Credits	4	**Exam. Duration**	3 Hours

Course objective is to:

- Understand the various techniques of sorting and searching
- Design and implement arrays, stacks, queues, and linked lists
- Understand the complex data structures such as trees and graphs

Module-1	**L1,L2,L3**	**12 Hours**

Basic Terminologies: Elementary Data Organizations, Data Structure Operations: insertion, deletion, traversal etc.; Analysis of an Algorithm, Asymptotic Notations, Time-Space trade off. Searching: Linear Search and Binary Search Techniques and their complexity analysis.

Laboratory Sessions/ Experimental learning:

- Implementation of searching Techniques

Applications: Array data type used in a programming language to specify a variable that can be indexed. Array data structure is used for arrangement of items at equally spaced and sequential addresses in computer memory makes it easier to perform operations like sorting, merging, traversal, retrievals

Video link / Additional online information :
https://www.tutorialspoint.com/data_structures_algorithms/array_data_structure.htm

Module-2	**L1,L2,L3**	**12 Hours**

ADT Stack and its operations: Algorithms and their complexity analysis, Applications of Stacks: Expression Conversion and evaluation – corresponding algorithms and complexity analysis. ADT queue, Types of Queue: Simple Queue, Circular Queue, Priority Queue; Operations on each types of Queues: Algorithms and their analysis.

Laboratory Sessions/ Experimental learning:

- Stack ADT to perform push and pop operations.
- Stack ADT for Expression Evaluation
- Array Implementation of Queue ADT

Applications: Expression Handling , Backtracking Procedure

Video link / Additional online information :
https://www.tutorialspoint.com/data_structures_algorithms/stack_algorithm.htm
https://www.tutorialspoint.com/data_structures_algorithms/dsa_queue.htm

Module-3	L1,L2,L3	12 Hours

Singly linked lists: Representation in memory, Algorithms of several operations: Traversing, Searching, Insertion into, Deletion from linked list; Linked representation of Stack and Queue, Header nodes, Doubly linked list: operations on it and algorithmic analysis; Circular Linked Lists: all operations their algorithms and the complexity analysis

Laboratory Sessions/ Experimental learning:

- Implementation of linked list techniques(SLL,DLL,CLL)

Applications: The cache in your browser that allows you to hit the BACK button where a linked list of URLs can be implemented. A linked list would be a reasonably good choice for implementing a linked list of file names, undo functionality in Photoshop

Video link / Additional online information :
https://www.tutorialspoint.com/data_structures_algorithms/linked_list_algorithms.htm
https://www.tutorialspoint.com/data_structures_algorithms/doubly_linked_list_algorithm.htm

Module-4	L1,L2,L3	12 Hours

Basic Tree Terminologies, Different types of Trees: Binary Tree, Threaded Binary Tree, Binary Search Tree, AVL Tree; Tree operations on each of the trees and their algorithms with Complexity analysis. Applications of Binary Trees. B Tree, B+ Tree: definitions, algorithms and analysis.

Laboratory Sessions/ Experimental learning:

- Develop a program to create a Binary Search Tree and to Traverse the tree.

Applications: Store hierarchical data, like folder structure, organization structure, XML/HTML data. Binary Search Tree is a tree that allows fast search, insert, delete on a sorted data. It also allows finding closest item. Heap is a tree data structure which is implemented using arrays and used to implement priority queues.

Video link / Additional online information :
https://www.tutorialspoint.com/data_structures_algorithms/tree_data_structure.htm
https://www.tutorialspoint.com/data_structures_algorithms/binary_search_tree.htm

Module-5	L1,L2,L3	12 Hours

Introduction to graph – types of graphs - Graph representations - Traversal algorithms- Depth First Search (DFS) and Breadth First Search (BFS) - Shortest path algorithms, Transitive closure, Minimum Spanning Tree, Topological sorting.

Laboratory Sessions/ Experimental learning:

- Implement shortest path Algorithms

Applications: The link structure of a website could be represented by a directed graph: the vertices are the web pages available at the website and a directed edge from page A to page B exists if and only if A contains a link to B. Graph colouring concept can be applied in job scheduling problems of CPU, jobs are assumed as vertices of the graph and there will be an edge between two jobs that cannot be executed simultaneously and there will be one-one relationship between feasible scheduling of graphs.

Video link / Additional online information :
https://www.tutorialspoint.com/data_structures_algorithms/graph_data_structure.htm

Course outcomes:	
CO1	Implement all the operations of linear data structures to store and retrieve the given data.
CO2	Create a hierarchical data structure to represent the given data using tree data structure.
CO3	Compare efficiency of various searching techniques using different tree data structures.
CO4	Apply stack, Queue, Lists, Trees and Graph concepts in problem solving
CO5	Implement all data structures in a high-level language for problem solving

Reference Books:	
1.	Seymour Lipschutz and Vijayalakshmi Pai G A, ―Data Structures‖, Tata McGraw Hill, New Delhi, 2013.
2.	Ellis Horowitz, Sartaj Sahni, Susan Anderson Freed, Fundamentals of Data Structures in C, Second Edition, Universities Press, 2008.
3.	Mark Allen Weiss, Data Structures and Algorithm Analysis in C, Second Edition, Pearson Education, 2015

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	3	0	0	0	0	2	0	0
CO2	3	3	3	2	3	0	0	0	0	2	0	0
CO3	3	3	2	2	3	0	0	0	0	2	0	0
CO4	3	3	2	2	3	0	0	0	0	2	0	0
CO5	3	3	3	2	3	0	0	0	0	2	0	0

High-3, Medium-2, Low-1

Course Title	Analog and Digital Electronics	**Semester**	III
Course Code	MVJ19IS33	**CIE**	50
Total No. of Contact Hours	60 L: T : P :: 40 : 0 : 20	**SEE**	50
No. of Contact Hours/week	3	**Total**	100
Credits	3	**Exam. Duration**	3 Hours

Course objective is to:

- Analyse the working of oscillators and use of regulators.
- Make use of simplifying techniques in the design of combinational circuits.
- Illustrate combinational and sequential digital circuits.
- Demonstrate the use of flipflops and design registers and counters.
- Design and test Analog-to-Digital and Digital-to-Analog conversion techniques.

Module-1	**L1,L2,L3**	**12 Hours**

Metal Oxide Semiconductor Field Effect transistor(MOSFET): Structure and I-V characteristics, MOSFET as a switch, MOSFET as an amplifier, CMOS and its applications.
Oscillators: Basic working and applications of RC Phase shift oscillator, Wien Bridge oscillator, LC oscillator, Colpitt oscillator, Crystal Oscillator.
Linear Power Supplies: Constituents of a Linear Power Supply, Designing Mains Transformer, Linear IC voltage regulators, Regulated Power Supply Parameters

Laboratory Sessions/ Experimental learning:

- Plotting the V-I characteristics of MOSFET

Applications:
FET,s are the basic elements in constructing memory devices. Oscillators' gives an ides of generating clock signals. Regulated power supplies help in regulating power in electronic products.

Video link / Additional online information :
https://www.youtube.com/watch?v=lNuS8mddhs0

Module-2	**L1,L2,L3**	**12 Hours**

Karnaugh maps: Minimum forms of switching functions, two and three variable Karnaugh maps, four variable karnaugh maps, Quine-McClusky Method: determination of prime implicants, The prime implicant chart, petricks method, simplification of incompletely specified functions, simplification using map-entered variables,

Laboratory Sessions/ Experimental learning:

- Writing and Analysing C program for K-maps.

Applications: Karnaugh maps are used for many small design problems. It gives a great deal of insight to digital logic circuits.

Video link / Additional online information :
https://nptel.ac.in/content/storage2/nptel_data3/html/mhrd/ict/text/106105185/lec20.pdf-

Module-3	L1,L2,L3	12 Hours

Combinational Circuits: Multiplexer, Decoders, Adders, Subtractors, BCD arithmetic, carry look ahead adder, serial adder, ALU-Design and popular MSI chips, digital comparator, parity checker/generator, code converters, priority encoders, decoders/drivers for display devices

Laboratory Sessions/ Experimental learning:

- Designing a 32-bit ALU

Applications: These components are used as a fundamental element in processor, communication devices etc.

Video link / Additional online information :
https://nptel.ac.in/content/storage2/nptel_data3/html/mhrd/ict/text/106102062/lec11.pdf

Module-4	L1,L2,L3	12 Hours

Flip-Flops and Registers: Flip Flops: S-R,J-K,D and T flip flops, Edge-triggered JK FLIP-FLOPs Registers: Types of Registers, Serial In - Serial Out, Serial In - Parallel out, Parallel In - Serial Out, Parallel In - Parallel Out, Universal Shift Register, Applications of Shift Registers. Counters: Asynchronous Counters, Decoding Gates, Synchronous Counters, Changing the Counter Modulus, Decade Counters, Applications of Counters.

Laboratory Sessions/ Experimental learning:

- Implementing 2-digit counters using seven segment display

Applications: Registers are use in processors for performing operations. Counters are used as Digital clocks, Frequency counters, Binary counters etc.

Video link / Additional online information :
https://www.youtube.com/watch?v=Gc3DL-tmr-g

Module-5	L1,L2,L3	12 Hours

D/A Conversion and A/D Conversion:
Digital to analog converters: weighted resistor/converter, R-2R Ladder D/A converter, specifications for D/A converters, examples of D/A converter lCs, sample and hold circuit.
Analog to digital converters: quantization and encoding, parallel comparator A/D converter, successive approximation A/D converter, counting A/D converter, dual slope A/D converter, A/D

converter using voltage to frequency and voltage to time conversion, specifications of A/D converters, example of A/D Converter ICs

Laboratory Sessions/ Experimental learning:

- Demonstration of CODEC which houses both ADC and DAC.

Applications: DACs are commonly used in music players to convert digital data streams into analog audio signals. They are also used in televisions and mobile phones to convert digital video data into analog video signals.ADCs are used in music recording, Digital signal processing, Scientific Instruments etc.

Video link / Additional online information :
https://www.youtube.com/watch?v=wa7pIviT-do-

Course outcomes:	
CO1	Design and analyse analog circuits using transistors, power supply, MOSFETS,regulator IC and opamp.
CO2	Simplify digital circuits using Karnaugh Map , POS and Quine-McClusky Methods
CO3	Explain construction and working of data processing circuits
CO4	Understanding the various types of latches and flip flops and building the registers and counters using flip flops.
CO5	Explain the basic principles of A/D and D/A conversion circuits and develop the same.

Reference Books:	
1.	Anil K Maini, Varsha Agarwal, Electronic Devices and Circuits, Wiley, 2012.
2.	Charles H Roth and Larry L Kinney, Fundamentals of Logic design, Cengage Learning,2019.
3.	Donald P Leach, Albert Paul Malvino & Goutam Saha, Digital Principles and Applications, 8th Edition, Tata McGraw Hill, 2015.
4	M. Morris Mani, Digital Design, 4th Edition, Pearson Prentice Hall, 2008.
5	David A. Bell, Electronic Devices and Circuits, 5th Edition, Oxford University Press, 2008

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2	2	0	0	0	0	0	0	0	1
CO2	3	3	2	2	0	0	0	0	0	0	0	1
CO3	3	3	3	2	0	0	0	0	0	0	0	1
CO4	3	3	2	2	0	0	0	0	0	0	0	1
CO5	3	3	3	2	0	0	0	0	0	0	0	1

High-3, Medium-2, Low-1

Course Title	Data Communication	**Semester**	III
Course Code	MVJ19IS34	**CIE**	50
Total No. of Contact Hours	60 L: T : P :: 40 : 0 : 20	**SEE**	50
No. of Contact Hours/week	3	**Total**	100
Credits	3	**Exam. Duration**	3 Hours

Course objective is to:

- Discuss the digital data communication techniques.
- Gain knowledge on basic concepts of data communication layers, protocols and performance.
- Understand a few representative protocols and network components.
- Introduce the functions of different layers from deployed examples.
- Introduce standards employed in computer networking.

Module-1	**L1,L2,L3**	**12 Hours**

Data Communications, Networks, The Internet, Protocol sand standards, Network Models-Reference models OSI, TCP/IP Model, Addressing, Data &Signal-Analog and Digital, Periodic Analog Signals, Digital Signals, Transmission impairment, Data Rate Limits, Performance.

Laboratory Sessions/ Experimental learning:

- Write a code simulating PING and TRACEROUTE commands

Applications: Resource sharing such as printers and storage devices.

Video link / Additional online information :
http://nptel.ac.in/courses/106105082/

Module-2	**L1,L2,L3**	**12 Hours**

Digital to Digital Conversions, Analog to Digital Conversions, Transmission Modes, Analog Transmission-Digital to Analog conversion, Analog to Analog conversion, Multiplexing- FDM, WDM, STDM, Statistical TDM, Spread Spectrum, Guided Media-Twisted pair cable, Co-axial cable, Fiber optic cable, Unguided media-Wireless-Radio waves, Microwaves, Infrared.

Laboratory Sessions/ Experimental learning:

- Create a socket for HTTP for web page upload and download.

Applications: Cellular telephony, video conferencing, digital TV

Video link / Additional online information :
http://nptel.ac.in/video.php?subjectId=106105081

Module-3	**L1,L2,L3**	**12 Hours**

Circuit switched networks, Datagram networks, Virtual circuit networks, Structure of a Switch-Structure of Circuit Switches & Packet Switches, Data Link Layer-Detection and Correction-

Introduction, Block Coding-Error Detection and Correction, Hamming Distance, Minimum Hamming Distance, Linear Block Codes, Cyclic Codes- CRC, Polynomials, Checksum.

Laboratory Sessions/ Experimental learning:

- Applications using TCP and UDP Sockets like

a. DNS
b. SNMP
c File Transfer

Applications: Connection between different devices using logical connections

Video link / Additional online information :
http://www.computerscienceonline.org/courses/

Module-4	**L1,L2,L3**	**12 Hours**

Data Link Layer – Data Link Control- Framing, Flow and error control, Protocols, Noiseless Channels, Noisy Channels, HDLC, Point-to-Point Protocol- Framing, Transition phases, Multiple Access- Random access-Aloha, CSMA, CSMA/CD, CSMA/CA, Controlled access- reservation, polling, token passing, Channelization - FDMA,TDMA,CDMA.

Laboratory Sessions/ Experimental learning:

- Implementation of Stop and Wait Protocol and Sliding Window Protocol.

Applications: media access control (MAC) layer, source and destination addresses

Video link / Additional online information :
https://www.youtube.com/view_play_list?p=32DBC269EF768F74

Module-5	**L1,L2,L3**	**12 Hours**

Wired LANs: Ethernet – Standard Ethernet, Fast Ethernet, Gigabit Ethernet, Wireless LANs- IEEE 802.11, Bluetooth - Architecture, Bluetooth layers, Radio layer, Baseband layer, L2CAP Connecting Devices–Hub, Repeater, Bridges, Transparent Bridges, Switches, Router, and Gateway.

Laboratory Sessions/ Experimental learning:

- Study of Network simulator (NS).and Simulation of Congestion Control Algorithms using NS

Applications: Internet Access.

Video link / Additional online information :
https://nptel.ac.in/courses/106105082/#

Course outcomes:	
CO1	Analyze OSI and TCP network models and the layers associated functionalities
CO2	Analyze and apply different types of signal conversion techniques in physical layer

CO3	Analyze and apply different types of error detection and correction mechanisms.
CO4	Analyze flow control and Error control mechanism using standard data link layer protocols and Compare different categories of Medium Access protocols
CO5	Analyze different protocols used for Ethernet and various connecting devices used in networks.

Reference Books:	
1.	Data Communication and Networking,BehrouzA.Forouzan,McGrawHill, 5thEdition,2012.
2.	Data and Computer Communication, WilliamStallings,10th Edition,PearsonEducation,2014.
3.	Introduction to Data Communications and Networking–Wayne Tomasi, Pearson Education,2009.(Latest Edition)

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	0	3	3	0	0	0	0	0	0	0	0	2
CO2	0	0	3	2	0	0	0	0	0	0	0	2
CO3	0	3	3	0	0	0	0	0	0	0	0	2
CO4	0	0	3	0	0	0	0	0	0	0	0	2
CO5	0	3	2	0	0	0	0	0	0	0	0	2

High-3, Medium-2, Low-1

Course Title	Computer Organization & Architecture	**Semester**	III
Course Code	MVJ19IS35	**CIE**	50
Total No. of Contact Hours	60 L: T : P :: 40 : 0 : 20	**SEE**	50
No. of Contact Hours/week	3	**Total**	100
Credits	3	**Exam. Duration**	3 Hours

Course objective is to:

- distinguish between the various ISA styles
- trace the execution sequence of an instruction through the processor
- compare different approaches used for implementing a functional unit
- understand the fundamentals of memory and I/O systems and their interaction with the processor

Module-1	**L1,L2,L3**	**12 Hours**

Functional unit, Basic operational concepts, Bus structures, Software, Performance, Data Representation. Fixed Point Representation. Floating – Point Representation. Instruction codes. Computer Registers Computer instructions– Instruction cycle. Memory – Reference Instructions. Input – Output and Interrupt. STACK organization. Instruction formats. Addressing modes.

Laboratory Sessions/ Experimental learning:

- Familiarization with assembly language programming

Applications: Computer system.

Video link / Additional online information :
https://nptel.ac.in/courses/106/106/106106166/

Module-2	**L1,L2,L3**	**12 Hours**

Peripheral Devices, Input-Output Interface, Asynchronous data transfer Modes of Transfer, Priority Interrupt Direct memory Access, Input –Output Processor (IOP) Serial communication; Introduction to peripheral component, Interconnect (PCI) bus. Introduction to standard serial communication protocols like RS232, USB, IEEE1394

Laboratory Sessions/ Experimental learning:

- Interfacing - DAC, ADC, keyboard-display modules

Applications: Monitors, keyboards.

Video link / Additional online information:
https://drive.google.com/file/d/0B-ITW-kTxwdfSVExbzZlMUFFVFU/view

Module-3	L1,L2,L3	12 Hours
Cache Coherence, Shared Memory Multiprocessors. Control memory, Address sequencing, micro program example, design of control unit Hard wired control. Micro programmed control, Virtual Memory. Laboratory Sessions/ Experimental learning: • Processor design Applications: High end workstations. Video link / Additional online information: https://drive.google.com/file/d/0B-ITW-kTxwdfcV9ma2JxbUc0RUk/view		

Module-4	L1,L2,L3	12 Hours
Addition and subtraction, multiplication Algorithms, Division Algorithms, Floating – point Arithmetic operations. Decimal Arithmetic unit Decimal Arithmetic operations. Laboratory Sessions/ Experimental learning: • Implementation of booth algorithm Applications: Radar,Sonar Video link / Additional online information: https://nptel.ac.in/courses/106/106/106106166/		

Module-5	L1,L2,L3	12 Hours
Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline, Data hazards – Instruction hazards, Vector Processing, Array Processors. Cache coherence and MESI protocol – Clusters – Non-Uniform Memory Access – Vector Computation Laboratory Sessions/ Experimental learning: • Introduction to embedded system. Applications: DSP,Microprocessor Video link / Additional online information: https://drive.google.com/file/d/0B-ITW-kTxwdfNGlMQlNSSVlQeEE/view		

Course outcomes:	
CO1	Demonstrate the fundamental organization of a computer system
CO2	Analyse various issues related to memory hierarchy.

CO3	Examine various, inter connection structures of multi processors.
CO4	Formulate and solve problems related to computer arithmetic, performance of systems
CO5	Demonstrate parallel computing and concepts of pipeline

Reference Books:	
1.	M. Morris Mano, Computer System Architecture, 3rd edition, Prentice- Hall of IndiaPvt. Ltd., 1999.
2.	Carl Hamacher : “Computer Organization ”, Fifth Edition, Mc Graw Hill
3.	William Stallings: “Computer Organisation and Architecture”, Pearson Education

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	0	0	3	2	0	0	0	2	0	0	0	1
CO2	0	3	3	2	0	0	0	2	0	0	0	2
CO3	0	3	3	2	0	0	0	2	0	0	0	3
CO4	0	3	3	2	0	0	0	2	0	0	0	2
CO5	0	3	3	2	0	0	0	2	0	0	0	3

High-3, Medium-2, Low-1

Course Title	Software Engineering	**Semester**	III
Course Code	MVJ19IS36	**CIE**	50
Total No. of Contact Hours	60 L: T : P :: 40 : 0 : 20	**SEE**	50
No. of Contact Hours/week	3	**Total**	100
Credits	3	**Exam. Duration**	3 Hours

Course objective is to:

- To understand the phases in a software project
- To understand fundamental concepts of requirements engineering and Analysis Modeling.
- To understand the various software design methodologies
- To learn various testing and maintenance measures

Module-1	**L1,L2, L3**	**12 Hours**

What is software engineering? Software Development Life Cycle, Essential characteristics of socio technical systems, Emergent System Properties, Systems Engineering, Functional and Non-functional requirements, User Requirements, System Requirements, Interface Specification, Documentation of the software requirements, Feasibility study, Requirements elicitation and analysis, Requirements Validations, Requirements Management.

Laboratory Sessions/ Experimental learning:

- Identifying the Requirements from Problem Statements

Applications: Software Project

Video link / Additional online information :
https://nptel.ac.in/courses/106/105/106105182/
http://vlabs.iitkgp.ernet.in/se/

Module-2	**L1,L2, L3**	**12 Hours**

Process and Project, Component Software Processes, Software Development Process Models: Waterfall Model, Prototyping, Spiral model, Iterative Development, Rational Unified Process, The RAD Model, Time boxing Model.
Rapid Software Development: Agile methods; Plan-driven and agile development, Extreme programming

Laboratory Sessions/ Experimental learning:

- Demonstration of Process Models

Applications: Software Project

Video link / Additional online information :

https://nptel.ac.in/courses/106/105/106105182/
http://vlabs.iitkgp.ernet.in/se/

Module-3	L1,L2, L3	12 Hours

Design process – Design Concepts-Design Model– Design Heuristic – Architectural Design – Architectural styles, Architectural Design, Architectural Mapping using Data Flow- User Interface Design: Interface analysis, Interface Design –Component level Design: Designing Class based components, traditional Components

Laboratory Sessions/ Experimental learning:

- Modeling UML Use Case Diagrams and Capturing Use Case Scenarios

Applications: System Design

Video link / Additional online information :
https://nptel.ac.in/courses/106/105/106105182/
http://vlabs.iitkgp.ernet.in/se/

Module-4	L1,L2, L3	12 Hours

Software testing fundamentals-Internal and external views of Testing-white box testing - basis path testing-control structure testing-black box testing- Regression Testing – Unit Testing – Integration Testing – Validation Testing – System Testing and Debugging.

Laboratory Sessions/ Experimental learning:

- Designing Test Suites.

Applications: System Testing

Video link / Additional online information :
https://nptel.ac.in/courses/106/105/106105182/
http://vlabs.iitkgp.ernet.in/se/

Module-5	L1,L2, L3	12 Hours

Software Implementation Techniques: Coding Practices, Refactoring, Maintenance and Reengineering-BPR model-Reengineering process model-Reverse and Forward Engineering.
Software Project Management: Estimation – LOC, FP Based Estimation, Make/Buy Decision COCOMO I & II Model .

Laboratory Sessions/ Experimental learning:

- Cost estimation of Project

Applications: Successful development of the project's procedures of initiation, planning, execution, regulation and closure

Video link / Additional online information :

https://nptel.ac.in/courses/106/105/106105182/ http://vlabs.iitkgp.ernet.in/se/

Course outcomes:	
CO1	Identify the key activities in software engineering
CO2	Compare different process models.
CO3	Apply requirements engineering process and analysis modeling.
CO4	Apply systematic procedure for software design and deployment.
CO5	Compare and contrast various testing techniques and apply software implementation techniques

Reference Books:	
1.	Roger S. Pressman, "Software Engineering – A Practitioner‟s Approach", Seventh Edition, Mc Graw-Hill International Edition, 2010.
2.	Ian Sommerville, "Software Engineering", 9th Edition, Pearson Education Asia, 2011.
3.	Rajib Mall, "Fundamentals of Software Engineering", Third Edition, PHI Learning Private Limited, 2009.
4.	Pankaj Jalote, "Software Engineering", Narosa Publication

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	0	0	2	0	0	0	0	0	0	0	0	0
CO2	2	2	0	0	0	0	0	0	0	0	0	0
CO3	2	0	1	0	3	0	0	0	0	0	0	0
CO4	2	2	0	2	0	1	0	1	0	0	3	3
CO5	1	2	0	0	0	0	0	0	0	0	0	3

High-3, Medium-2, Low-1

Course Title	Data Structure Lab	**Semester**	III
Course Code	MVJ19ISL37	**CIE**	50
Total No. of Contact Hours	40 L: T: P: 0: 0: 40	**SEE**	50
No. of Contact Hours/week	4	**Total**	100
Credits	2	**Exam. Duration**	3 Hours

Course objective is to:

- Implement linear and non-linear data structures
- Understand the different operations of search trees
- Implement graph traversal algorithms
- Get familiarized to sorting and searching techniques

Sl No	Experiment Name	RBT Level	Hours
1	Implementation of searching algorithms a) Linear Search b) Binary Search	L3	4
2	Implementation of sorting algorithms a) Insertion sort b) Selection sort c) Quick sort d) Merge sort	L3	4
3	a) Array implementation of List ADT b) Linked list implementation of List ADT	L3	4
4	a) Array implementation of Stack ADT b) Linked list implementation of Stack ADT	L3	4
5	a) Array implementation of queue ADT b) Linked list implementation of queue ADT	L3	4
6	Program to create a Binary Search Tree and to traverse the tree.	L3	4
7	Program to compute the shortest path from a single source	L3	4
8	Program to construct a graph and perform graph traversal (BFS, DFS)	L3	4
9	Program to construct a minimum spanning tree using: a) Prims Algorithm b) Kruskal's Algorithm	L3	4
10	Development of a Mini project/Present a case Study	L3	4

Course outcomes:	
CO1	Compute the time and space complexity of searching and sorting algorithms with asymptotic notations.
CO2	Implement all the operations of linear data structures to store and retrieve the given data.
CO3	Apply Algorithm for solving problems like sorting, searching, insertion and deletion of data
CO4	Create a hierarchical data structure to represent the given data using tree data structure.
CO5	Design graph algorithms to compute the shortest path of the given graph and to identify the Minimum spanning tree.

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	3	0	0	0	0	2	0	0
CO2	3	3	3	2	3	0	0	0	0	2	0	0
CO3	3	3	2	2	3	0	0	0	0	2	0	0
CO4	3	3	2	2	3	0	0	0	0	2	0	0
CO5	3	3	3	2	3	0	0	0	0	2	0	0

High-3, Medium-2, Low-1

Course Title	Analog & Digital Electronics Lab	**Semester**	III
Course Code	MVJ19ISL38	**CIE**	50
Total No. of Contact Hours	40 L: T: P: 0: 0: 40	**SEE**	50
No. of Contact Hours/week	4	**Total**	100
Credits	2	**Exam. Duration**	3 Hours

Course objective is to:

- Analog components and circuits including transistor, regulator, etc.
- Combinational logic circuits.
- Flip - Flops and their operations
- Counters and Registers using Flip-flops.
- Synchronous and Asynchronous Sequential Circuits

Sl No	Experiment Name	RBT Level	Hours
1	Study of transistor phase shift oscillator and observe the effect of variation in R & C on oscillator frequency and compare with theoretical value.	L3	3
2	Design and test IC 723 voltage regulator	L3	3
3	Given a 4-variable logic expression, simplify it using Entered Variable Map and realize the simplified logic expression using 8:1 multiplexer IC.	L3	3
4	Design and implement a faster way3 to add binary numbers using carry look ahead adders.	L3	3
5	A) Realization and implementation of 2-bit comparator using logic gates. b) Implementation of 4-bit magnitude comparator using IC 7485.	L3	3
6	To design and construct basic flip-flops R-S ,J-K,J-K Master slave flip-flops using gates and verify their truth table	L3	3
7	Implementation of SISO, SIPO, PISO and PIPO shift registers using Flip- flops	L3	4
8	Design and implementation of 3-bit synchronous up/down counter	L3	4
9	Design and implement a ring counter and Johnson counter using 4-bit shift register and demonstrate its working.	L3	3
10	Design and implement a mod-n (n<8) synchronous up counter using J-K Flip-Flop ICs and demonstrate its working.	L3	4
11	Design and implement an asynchronous counter using decade counter IC to count up from 0 to n (n<=9) and demonstrate on 7-segment display (using IC-7447).	L3	3
12	Design 4 bit R-2R ladder DAC using opamp.	L3	4

Course outcomes:	
CO1	Demonstrate various Electronic Devices like Cathode ray Oscilloscope, Signal generators, Digital Trainer Kit, Multimeters and components like Resistors, Capacitors, Op amp and Integrated Circuit
CO2	Examine and verify different analog circuits.
CO3	Design and demonstrate various combinational logic circuits.
CO4	Design and demonstrate various types of counters and Registers using Flip-flops
CO5	Design and demonstrate the working of DAC

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2	2	0	0	0	0	0	0	0	0
CO2	3	3	2	2	0	0	0	0	0	0	0	0
CO3	3	3	3	2	0	0	0	0	0	0	0	0
CO4	3	3	2	2	0	0	0	0	0	0	0	0
CO5	3	3	3	2	0	0	0	0	0	0	0	0

High-3, Medium-2, Low-1