| Advanced Engineering Mathematics | | Semester | 1 |
|---|---|---|---|
| Course Code | **MVJ22XXX11** | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | **L: T:P:S: 3:0:0:0** | SEE Marks | 50 |
| Total Hours of Pedagogy | **40L** | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |
| Examination type (SEE) | Theory | | |

**Course Objectives:**

- Apply discrete and continuous probability distributions in analyzing the probability models arising in engineering field.
- Learn the mathematical formulation of linear programming problem.
- Learn the mathematical formulation of transportation problem.
- Understand the concepts of Complex variables and transformation for solving Engineering Problems.
- Learn the solutions of partial differential equations numerically.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

**Module-1**

**Linear Algebra-I:** Introduction to vector spaces and sub-spaces, definitions, illustrative example. Linearly independent and dependent vectors- Basis-definition and problems. Linear transformations-definitions. Matrix form of linear transformations-Illustrative examples (Text Book:1).

**Module-2**

**Linear Algebra-II:** Computation of eigen values and eigen vectors of real symmetric matrices-Given's method. Orthogonal vectors and orthogonal bases. Gram-Schmidt orthogonalization process (Text. Book:1)

**Module-3**

**Calculus of Variations:** Concept of functional- Eulers equation. Functional dependent on first and higher order derivatives, Functional on several dependent variables. Isoperimetric problems-variation problems with moving boundaries. (Text.Book:2)

**Module-4**

**Probability Theory:** Review of basic probability theory. Definitions of random variables and probability distributions, probability mass and density functions, expectation, moments, central moments, characteristic functions, probability generating and moment generating functions-illustrations. Poisson, Gaussian and Erlang distributions examples. (Text Book: 3)

**Module-5**

**Engineering Applications on Random processes:** Classification. Stationary, WSS and ergodic random process. Auto-correlation function - properties, Gaussian random process. (Text Book: 3)

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

1. Understand vector spaces, basis, linear transformations and the process of obtaining matrix of linear transformations arising in magnification and rotation of images.
2. Apply the technique of singular value decomposition for data compression, least square approximation in solving inconsistent linear systems
3. Utilize the concepts of functional and their variations in the applications of communication systems, decision theory, synthesis and optimization of digital circuits.
4. Learn the idea of random variables (discrete/continuous) and probability distributions in analyzing the probability models arising in control systems and system communications.
5. Analyze random process through parameter-dependent variables in various random processes.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Books**


1. David C.Lay, Steven R. Lay and J.J.McDonald, "Linear Algebra and its Applications", Pearson Education Ltd., 5th Edition, 2015
2. E. Kreyszig, "Advanced Engineering Mathematics", Wiley, 10th edition, 2015
3. Scott L.Miller, Donald G. Childers, "Probability and Random Process with application to Signal Processing", Elsevier Academic Press, 2nd Edition, 2013


**Web links and Video Lectures (e-Resources):**

- http://www.digimat.in/nptel/courses/video/111106051/L01.html
- https://archive.nptel.ac.in/courses/111/104/111104025/
- https://archive.nptel.ac.in/courses/111/104/111104079/

| VLSI DESIGN WITH VERILOG | | Semester | 1 |
|---|---|---|---|
| Course Code | **MVJ22LVL12** | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 3:0:2:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 Hours Theory + 10-12 Lab Slots | Total Marks | 100 |
| Credits | 04 | Exam Hours | 3+3 |
| Examination nature (SEE) | Theory and Practical | | |

**Course objectives:**

- To understand the operation of MOS transistor, Scaling and Small Geometry Effects.
- Realization of the basic IC design concepts.
- To study Static Characteristics, Switching Characteristics and Interconnect Effect of MOS Inverter.
- To provide the insight of Semiconductor Memories, Dynamic Logic Circuits and BiCMOS Logic Circuits.

**Teaching-Learning Process (General Instructions)**
These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

**MODULE-1**

**MOS Transistor:** The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small- Geometry Effects.

**MOS Inverters-Static Characteristics:** Introduction, Resistive-Load Inverter, Inverters with n_Type MOSFET Load

**MODULE-2**

**MOS Inverters-Static Characteristics:** CMOS Inverter.

**MOS Inverters:** Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitics, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters.

**MODULE-3**

**Semiconductor Memories:** Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM)

**Basic BiCMOS Circuits:** Static Behavior, Switching Delay in BiCMOS Logic Circuits,BiCMOS Applications.

**MODULE-4**

**Dynamic Logic Circuits:** Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS circuits

**MODULE-5**

**Basics of verilog : T**ypical HDL-flow, why Verilog IIDL?, trends in HDLs.

**Gate-Level Modeling:** Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays.

**Behavioral Modeling:** Structured procedures, initial and always, blocking and non- blocking statements, delay control, generate statement, event control, conditional statements, Multiway branching, loops, sequential and parallel blocks.

**PRACTICAL COMPONENT OF IPCC***(May cover all / major modules)*

| Sl.NO | Experiments |
|---|---|
| 1 | Write Verilog code for SR and verify the flip flop. |
| 2 | Write Verilog code for D and verify the flip flop. |
| 3 | Write Verilog code for JK and verify the flip flop |
| 4 | Write Verilog code for T and verify the flip flop. |
| 5 | Write Verilog code for MSJK and verify the flip flop. |
| 6 | Write Verilog code for counter with given input clock and check whether it works as clock divider performing division of clock by 2, 4, 8 and 16. |
| 7 | Verify the functionality of the code Model in Verilog for a full adder and add functionality to perform logical operations of XOR, XNOR, AND and OR gates. Write test bench with appropriate input patterns to verify the modeled behavior. |
| 8 | Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter with Wn = Wp, Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following:<br><br>i Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and time period of 20ns and plot the input voltage and output voltage of designed inverter?<br>ii. From the simulation results compute tpHL, tpLH and td for all three geometrical settings of width?<br>iii Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter? |

**Course outcomes (Course Skill Set):**

At the end of the course, the student will be able to:

- Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation.
- Analyse the Switching Characteristics in Digital Integrated Circuits.
- Use the Dynamic Logic circuits in state-of-the-art VLSI chips.
- Study critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon.
- Use Bipolar and Bi-CMOS circuits in very high speed design.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

**CIE for the theory component of the IPCC**

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

**CIE for the practical component of the IPCC**

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

**SEE for IPCC**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

5. The question paper will have ten questions. Each question is set for 20 marks.
6. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
7. The students have to answer 5 full questions, selecting one full question from each module.
8. Marks scored by the student shall be proportionally scaled down to 50 Marks

**The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component**.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Suggested Learning Resources:**

**Books**


1. **"**Sung Mo Kang & Yusuf Leblebici", CMOS Digital Integrated Circuits: Analysis and Design, Tata McGraw-Hill, Third Edition.
2. "Neil Weste and K. Eshraghian", Principles of CMOS VLSI Design: A System Perspective Pearson Education (Asia) Pvt. Ltd. Second Edition, 2000.
3. "Douglas A Pucknell& Kamran Eshraghian", Basic VLSI Design PHI 3rd Edition
4. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Pearson Education, Second Edition.


**Web links and Video Lectures (e-Resosurces):**

- http://www.nptelvideos.com/video.php?id=2431&c=4
- https://nptel.ac.in/courses/108106069
- https://nptel.ac.in/courses/108106158

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Design fast adders using verilog.
- Design multipliers using Verilog

| ADVANCED EMBEDDED SYSTEMS | | Semester | 1 |
|---|---|---|---|
| Course Code | **MVJ22LVL13** | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | **L:T:P: 3:0:0** | SEE Marks | 50 |
| Total Hours of Pedagogy | **40L** | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |
| Examination type (SEE) | Theory | | |

**Course objectives:**

- To understand basic concepts of Embedded Systems.
- To know development of Hardware Software co-design in Embedded System.
- To understand Architecture of ARM-32 bit Microcontroller.
- To analyse Instruction sets by Assembly basics, Instruction list and description.
- To learn Cortex-M3 programming using C language concepts and Microcontroller Software Interface Standard concepts.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

**Module-1**

**Embedded System:** Embedded vs General computing system, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Opto coupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems

**Module-2**

**Embedded System (Continued):** Hardware Software Co-Design, embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), Files generated during compilation, simulators, emulators and debugging

**Module-3**

**ARM-32 bit Microcontroller:** Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence .

**Module-4**

**Instruction Sets:** Assembly basics, Instruction list and description, useful instructions,

**Memory Systems:** Memory maps, Memory access attributes ,Default Memory Access Permissions ,Bit band operations ,Endian Mode .

**Module-5**

Exceptions, Nested Vector interrupt controller design, Systick Timer, Cortex-M3 Programming using assembly and C language, CMSIS .

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

1. Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
2. Explain the hardware software co-design and firmware design approaches.
3. Understand the suitability of the instruction sets of ARM processors to design of embedded systems.
4. Acquire the knowledge of the architectural features of ARM CORTEX M3, a 32-bit microcontroller including memory map, interrupts and exceptions.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

9. The question paper will have ten questions. Each question is set for 20 marks.
10. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

**Suggested Learning Resources:**

**Books**

1. K. V. Shibu , "Introduction to embedded systems", TMH education Pvt. Ltd. 2009

2. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, Newnes, (Elsevier) 2nd edn, 2010.
3. James K. Peckol , “Embedded systems - A contemporary design tool”, John Wiley, 2008

**Web links and Video Lectures (e-Resources):**

- https://nptel.ac.in/courses/108102045
- https://archive.nptel.ac.in/courses/106/105/106105193/
- https://archive.nptel.ac.in/courses/106/105/106105163/

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Assembly language programs to perform arithmetic and logical operations.
- Assembly language program to turn on/off LEDs
- Assembly language program to Interface ARM microcontroller with ADC,DAC,LCD etc

| VLSI TESTING | | Semester | I |
|---|---|---|---|
| Course Code | **MVJ22LVL14** | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | **L:T:P: 2:0:1:0** | SEE Marks | 50 |
| Total Hours of Pedagogy | **40L** | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |
| Examination type (SEE) | Theory | | |

**Course objectives:**

- To introduce VLSI testing.
- To introduce logic and fault simulation and testability measures.
- To study the test generation for combinational and sequential circuits
- To study the design for testability.
- To study the fault diagnosis.

**Teaching-Learning Process (General Instructions)**
These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

**Module-1**

**Faults in digital circuits:** Failures and Faults, Modeling of faults, Temporary Faults.

**Logic Simulation:** Applications, Problems in simulation based design verification, types of simulation, The unknown logic values, compiled simulation, event-driven simulation, Delay models, Element evaluation, Hazard Detection, Gate-level event-driven Simulation

**Module-2**

**Test generation for Combinational Logic circuits**: Fault Diagnosis of digital circuits, Test generation techniques for combinational circuits, Detection of multiple faults in Combinational logic circuits.

**Module-3**

**Testable Combinational logic circuit design:** Testable design of multilevel combinational circuits, Synthesis of random pattern testable combinational circuits, Path delay fault testable combinational logic design, Testable PLA design.

**Module-4**

**Design of testable sequential circuits:** Controllability and observability, Ad-Hoc design rules for improving testability, design of diagnosable sequential circuits, the scan-path technique for testable sequential circuit design, Level Sensitive Scan Design (LSSD), Random Access Scan Technique, Partial scan, testable sequential circuit design using Non scan Techniques, Cross check, Boundary Scan.

**Module-5**

Built-In Self Test: Test pattern generation for BIST, Output response analysis, Circular BIST, BIST Architectures.

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

1. Analyze the need for fault modelling and testing of digital circuits
2. Generate fault lists for digital circuits and compress the tests for efficiency
3. Apply the various techniques to enhance testability of combinational circuits
4. Apply boundary scan technique to validate the performance of digital circuits
5. Design built-in self-tests for complex digital circuits

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

13. The question paper will have ten questions. Each question is set for 20 marks.
14. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

**Suggested Learning Resources:**

**Books**

1. Lala Parag K," Digital Circuit Testing and Testability New York", Academic Press 1997 .

2. Abramovici M, Breuer M A and Friedman A “Digital Systems Testing and Testable Design” D Wiley 1994.
3. Vishwani D Agarwal” Essential of Electronic Testing for Digital, Memory and Mixed Signal Circuits” Springer 2002.
4. Wang, Wu and Wen Morgan” VLSI Test Principles and Architectures” Kaufmann, 2006.

**Web links and Video Lectures (e-Resources):**

- http://www.digimat.in/nptel/courses/video/117105137/L14.html
- https://archive.nptel.ac.in/courses/106/105/106105185/
- https://archive.nptel.ac.in/courses/117/106/117106092/

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Verilog/SystemVerilog program to find the functional coverage, code coverage etc.
- Verilog/SystemVerilog program to test a logic using BIST method.

| ASIC DESIGN | | Semester | 1 |
|---|---|---|---|
| Course Code | **MVJ22LVL15** | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | **L:T:P: 2:0:1:0** | SEE Marks | 50 |
| Total Hours of Pedagogy | **40L** | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |
| Examination type (SEE) | Theory | | |

**Course objectives:**

- To learn ASIC methodologies and programmable logic cells to implement a function on IC.
- To Analyse back-end physical design flow, including partitioning, floor-planning, placement, and routing.
- To Gain sufficient theoretical knowledge for carrying out FPGA and ASIC designs.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

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**Module-1**

**Introduction to ASICs:** Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries.

CMOS Logic: Data path Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers.

**Module-2**

.**ASIC Library Design:** Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages, library cell design.

**Programmable ASIC Logic Cells:** MUX as Boolean function generators, Acted ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA:XC3000 CLB, Altera FLEX and MAX, Programmable ASIC I/O Cells: Xilinx and Altera I/O Block.

**Module-3**

***Low-level design entry: Schematic entry:*** Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, vectored instances & buses, Edit in place, attributes, Netlist screener.

ASIC Construction: Physical Design, CAD Tools System partitioning, Estimating ASIC size.

**Partitioning:** Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms.

**Module-4**

**Floor planning and placement:** Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning.

**Placement:** Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow.

**Module-5**

**Routing:** Global Routing: Goals and objectives, Global Routing Methods, Global routing between blocks, Back- annotation. Detailed Routing: Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Area-Routing Algorithms, Multilevel routing, Timing –Driven detailed routing, Final routing steps, Special Routing, Circuit extraction and DRC.

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

1. Describe the concepts of ASIC design methodology, data path elements, logical effort.
2. Analyze the design of ASICs suitable for specific tasks, perform design entry and explain the physical design flow
3. Design data path elements for ASIC cell libraries and compute optimum path delay.
4. Create floor plan including partition and routing with the use of CAD algorithms.
5. Design CAD algorithms and explain how these concepts interact in ASIC design.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

17. The question paper will have ten questions. Each question is set for 20 marks.
18. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

**Suggested Learning Resources:**

**Books**


1. Michael John Sebastian Smith, "Application - Specific Integrated Circuits", Addison- Wesley Professional, 2005
2. Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", Addison Wesley/ Pearson education 3rdedition, 2011
3. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations" Springer, ISBN: 978-1-4614-1119-2. 2011
4. Rakesh Chadha, Bhasker J, "An ASIC Low Power Primer", Springer, ISBN: 978-14614-4270-7.

5. Peter J. Ashenden Digital Design (Verilog): An Embedded Systems Approach Using Verilog,1st Edition, Kindle Edition

**Web links and Video Lectures (e-Resources):**

- https://nptel.ac.in/courses/117106092
- https://archive.nptel.ac.in/courses/106/105/106105193/
- https://archive.nptel.ac.in/courses/106/105/106105161/

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Analyze the transistor behaviour and plot VI characteristics.
- Draw the analog architecture of inverter using suitable tool and analyze the characteristics for different $w_p/w_n$ values.

| RESEARCH METHODOLOGY AND IPR | | Semester | 1 |
|---|---|---|---|
| Course Code | **22RMI16** | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | **L:T:P: 3:0:0** | SEE Marks | 50 |
| Total Hours of Pedagogy | **40L** | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 s |
| Examination type (SEE) | Theory | | |

**Course objectives:**

This course will enable students:

• To give an overview of the research methodology and explain the technique of defining a research problem

• To explain the functions of the literature review in research.

• To explain carrying out a literature search, its review, developing theoretical and conceptual frameworks and writing a review.

• To explain various research designs and their characteristics.

• To explain the details of sampling designs, and also different methods of data collections.

• To explain the art of interpretation and the art of writing research reports.

• To explain various forms of the intellectual property, its relevance and business impact in the changing global business environment.

• To discuss leading International Instruments concerning Intellectual Property Rights

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

**Module-1**

**Research Methodology:** Introduction, Meaning of Research, Objectives of Research, Types of Research,Research Approaches, Significance of Research, Research Methods versus Methodology, Research and Scientific Method, Research Process, Criteria of Good Research, Problems Encountered by Researchers in India.

**Defining the Research Problem:** Research Problem, Selecting the Problem, Necessity of Defining the Problem,Technique Involved in Defining a Problem, An Illustration.

**Module-2**

**Reviewing the literature:** Place of the literature review in research, Bringing clarity and focus to research problem, Improving research methodology, Broadening knowledge base in research area, Enabling contextual findings, Review of the literature, searching the existing literature, reviewing the selected literature, Developing a theoretical framework, Developing a conceptual framework, Writing about the literature reviewed.

**Module-3**

**Design of Sample Surveys:** Design of Sampling: Introduction, Sample Design, Sampling and Non-sampling Errors, Sample Survey versus Census Survey, Types of Sampling Designs.

**Measurement and Scaling:** Qualitative and Quantitative Data, Classifications of Measurement Scales, Goodness of Measurement Scales, Sources of Error in Measurement, Techniques of Developing Measurement Tools, Scaling, Scale Classification Bases, Scaling Technics, Multidimensional Scaling, Deciding the Scale.

**Data Collection:** Introduction, Experimental and Surveys, Collection of Primary Data, Collection of Secondary Data, Selection of Appropriate Method for Data Collection, Case Study Method.

**Module-4**

**Testing of Hypotheses:** Hypothesis, Basic Concepts Concerning Testing of Hypotheses, Testing of Hypothesis, Test Statistics and Critical Region, Critical Value and Decision Rule, Procedure for Hypothesis Testing, Hypothesis Testing for Mean, Proportion, Variance, for Difference of Two Mean, for Difference of Two Proportions, for Difference of Two Variances, P-Value approach, Power of Test, Limitations of the Tests of Hypothesis.

**Chi-square Test:** Test of Difference of more than Two Proportions, Test of Independence of Attributes, Test of Goodness of Fit, Cautions in Using Chi Square Tests

**Module-5**

**Interpretation and Report Writing:** Meaning of Interpretation, Technique of Interpretation, Precaution in Interpretation, Significance of Report Writing, Different Steps in Writing Report, Layout of the Research Report, Types of Reports, Oral Presentation, Mechanics of Writing a Research Report, Precautions for Writing Research Reports. Intellectual Property: The Concept, Intellectual Property System in India, Development of TRIPS Complied.

**Course outcome (Course Skill Set)**

- At the end of the course, the student will be able to :
- Describe the concepts of ASIC design methodology, data path elements, logical effort.
- Analyze the design of ASICs suitable for specific tasks, perform design entry and explain the physical design flow
- Design data path elements for ASIC cell libraries and compute optimum path delay.
- Create floor plan including partition and routing with the use of CAD algorithms.
- Design CAD algorithms and explain how these concepts interact in ASIC design.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

21. The question paper will have ten questions. Each question is set for 20 marks.
22. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

**Suggested Learning Resources:**

**Books**


6. Michael John Sebastian Smith, "Application - Specific Integrated Circuits", Addison- Wesley Professional, 2005
7. Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", Addison Wesley/ Pearson education 3rdedition, 2011
8. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations" Springer, ISBN: 978-1-4614-1119-2. 2011
9. Rakesh Chadha, Bhasker J, "An ASIC Low Power Primer", Springer, ISBN: 978-14614-4270-7.

10. Peter J. Ashenden Digital Design (Verilog): An Embedded Systems Approach Using Verilog,1st Edition, Kindle Edition

**Web links and Video Lectures (e-Resources):**

- https://onlinecourses.nptel.ac.in/noc22_ge08/preview
- https://onlinecourses.nptel.ac.in/noc22_hs01/preview
- https://onlinecourses.nptel.ac.in/noc22_hs05/preview

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

-

| VLSI Design Lab-1 | | Semester | |
|---|---|---|---|
| Course Code | **MVJ22LVSL17** | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | **L: T:P:S: 1:0:1:0** | SEE Marks | 50 |
| Credits | 02 | Exam Hours | 100 |
| Examination type (SEE) | Practical | | |

**Course objectives:**

- . Understand the features of CAD tool in VLSI design.
- Design and verify the behavior of digital circuits using digital flow
- Synthesize the circuit in VLSI tool
- Verify the design using a logic analyzer
- Analyse physical design

**ASIC-Digital Design Flow**

**CADENCE/SYNOPSYS/MENTOR GRAPHICS/TANNER or any other equivalent Tool**

**PART-A**

Write Verilog Code for the following circuits and their Test Bench for verification, observe the wave technological library (constraints to be given). Do the initial timing verification with gate level simulation.

1.An inverter, Buffer, Transmission gate and basic gates
2.Flip flop - RS, D, JK, MS, T
3.4-bit counter [Synchronous & Asynchronous counter]

**FPGA DIGITAL DESIGN**

**FPGA/CPLD Boards with Xilinx or any other equivalent**

**PART-B**

1.Write Verilog code for the design of 8-bit
i.Carry Ripple Adder
ii.Carry Look Ahead adder
iii.Carry Skip Adder

2.Write Verilog Code for 8-bit
i.Array Multiplication (Signed and Unsigned)
ii.Booth Multiplication (Radix-4)

3.Write Verilog code for 4/8-bit
i.Magnitude Comparator
ii.LFSR
iii.Parity Generator
iv.Universal Shift Register

Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence. Eg 11101 (with and without overlap) any sequence can be specified.

**Course outcomes (Course Skill Set):**

At the end of the course the student will be able to:

- Understand the features of CAD tool in VLSI design.
- Design and verify the behavior of digital circuits using digital flow
- Synthesize the circuit in VLSI tool
- Verify the design using a logic analyzer
- Analyse physical design

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation (CIE):**

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry weightage of 60% and the rest 40% for viva-

**Semester End Evaluation (SEE):**

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.

- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

**Suggested Learning Resources:**

-

| VLSI PROCESSING TECHNOLOGY | | Semester | 2 |
|---|---|---|---|
| Course Code | MVJ22LVL21 | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | **L: T:P:S: 2:2:0:0** | SEE Marks | 50 |
| Total Hours of Pedagogy | **40L** | Total Marks | 100 |
| Credits | 3 | Exam Hours | 3 |
| Examination type (SEE) | Theory | | |

**Course objectives:**

- To understand the theoretical and practical aspect of very large scale integration
- To analyse doping profiles and material properties with SOI technology.
- To learn the art of lithography with different techniques.
- To analyse plasma discharge properties and the diagnostic techniques.
- To understand implantation process and applicability of metallization scheme.

**Teaching-Learning Process (General Instructions)**
These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

**Module-1**

**Crystal Growth and Wafer Preparation:** Introduction, Electronic-Grade Silicon, Czochralski Crystal Growing.

**Epitaxy:** Introduction, Vapour-Phase Epitaxy.

**Module-2**

**Lithography**: Introduction, Optical Lithography, Electron Lithography, X-ray Lithography, IonLithography.

**Module-3**

**Reactive Plasma Etching**: Introduction, Plasma Properties, Feature-Size Control and Anisotropic Etch Mechanisms, Other Properties of Etch Processes, Reactive Plasma-Etching Techniques and Equipment, Specific Etch Processes.

**Module-4**

**Ion Implantation**: Introduction, Range Theory, Implantation Equipment, Annealing, Shallow Junctions, High-Energy Implantation.

**Module-5**

**Metallization**: Introduction, Metallization Applications, Metallization Choices, Physical Vapor Deposition, Patterning, Metallization problems .

**Course outcomes (Course Skill Set):**
At the end of the course, the student will be able to:

1. Understand the major steps in the fabrication process of VLSI circuits.
2. Illustrate particular processing steps in achieving required parameters.
3. Apply standard engineering for different lithographic methods.
4. Analyse the specific plasma process used in semiconductor industry
5. Apply implantation process for VLSI devices and discuss the limitations of various metallization schemes..

## Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

**Suggested Learning Resources:**

**Books**


1. "S. M. Sze, "VLSI Technology", McGraw-Hill, Second Edition.
2. S.K. Ghandhi, "VLSI Fabrication Principles", John Wiley Inc., New York, 1994, Second Edition.


**Web links and Video Lectures (e-Resources):**

- https://archive.nptel.ac.in/courses/117/108/102108078/
- https://archive.nptel.ac.in/content/storage2/courses/103106075/Courses/Lecture15

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Analyze the transistor behaviour and plot VI characteristics.
- Draw the analog architecture of inverter using suitable tool and analyze the characteristics for different $w_p/w_n$ values.

| **DESIGN OF ANALOG AND MIXED MODE VLSI CIRCUITS** | | Semester | 2 |
|---|---|---|---|
| Course Code | MVJ22LVL22 | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | **L:T:P: 3:0:2:0** | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 Hours Theory + 10-12 Lab Slots | Total Marks | 100 |
| Credits | 04 | Exam Hours | 3+3 |
| Examination nature (SEE) | Theory and Practical | | |

**Course objectives:**

- To understand the basic physics and operation of MOS devices.
- To study Single-Stage and Differential Amplifiers.
- To learn Data Converter Specifications and Architectures.
- To understand Single ended Differential Amplifier and operations.
- To learn architecture of Data converter includes ADC (Analog to Digital) and DAC(Digital to Analog) Converters

**Teaching-Learning Process (General Instructions)**
These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

**MODULE-1**

**Basic MOS Device Physics**: General considerations, MOS I/V Characteristics, second order effects, MOS device models.

**MODULE-2**

**Single stage Amplifier**: Basic Concepts, Common Source stage, Source follower.

**MODULE-3**

**Single stage Amplifier**: common-gate stage, Cascode Stage, choice of device models.

**MODULE-4**

**Differential Amplifiers**: Single ended and differential operation, Basic differential pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

**MODULE-5**

**Data Converter Architectures**: DAC & ADC Specifications, Current Steering DAC, Charge Scaling DAC, Flash ADC, Successive Approximation ADC.

**PRACTICAL COMPONENT OF IPCC***(May cover all / major modules)*

| Sl.NO | Experiments |
|---|---|
| 1 | 1. Design an Inverter with given specifications*, completing the design flow mentioned below:<br>a. Draw the schematic and verify the following<br>i) DC Analysis<br>ii) Transient Analysis<br>b. Draw the Layout and verify the DRC, ERC<br>c. Check for XX<br>d. Extract RC and back annotate the same and verify the Design<br>e. Verify & Optimize for Time, Power and Area to the given Constraint |
| 2 | 2.Design the following circuits with given specifications*, completing the design flow mentioned below:<br>a. Draw the schematic and verify the following<br>i) DC Analysis<br>ii) AC Analysis<br>iii) Transient Analysis<br>b. Draw the Layout and verify the DRC, ERC, LVS<br>c. Check for XX<br>d. Extract RC and back annotate the same and verify the Design<br>i) Single Stage differential amplifier<br>ii) Common source amplifier |

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

- Use efficient analytical tools for quantifying the behavior of basic circuits by inspection.
- Design high-performance, amplifier circuits with the trade-offs between speed, precision and power dissipation.
- Design and study the behavior of phase-locked-loops for the applications.
- Identify the critical parameters that affect the analog and mixed-signal VLSI circuits' performance
- Perform calculations in the digital or discrete time domain, more sophisticated data converters to translate the digital data to and from inherently analog world.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

**CIE for the theory component of the IPCC**

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in

22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.

- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

**CIE for the practical component of the IPCC**

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

**SEE for IPCC**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

**The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component**.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Suggested Learning Resources:**

**Books**


1. "Behzad Razavi", Design of Analog CMOS Integrated Circuits, TMH 2007.
2. "R. Jacob Baker", CMOS Circuit Design, Layout, and Simulation, Wiley Second Edition
3. "Phillip E. Allen, Douglas R. Holberg", CMOS Analog Circuit Design Oxford University Press Second Edition.


**Web links and Video Lectures (e-Resources):**

- https://nptel.ac.in/courses/117107094
- https://nptel.ac.in/courses/117106034

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Analyze the transistor behaviour and plot VI characteristics.
- Draw the analog architecture of inverter using suitable tool and analyze the characteristics for different $w_p/w_n$ values.

| ADVANCES IN VLSI DESIGN | | Semester | 2 |
|---|---|---|---|
| Course Code | **MVJ22LVL231** | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | **L:T:P: 2:2:0:0** | SEE Marks | 50 |
| Total Hours of Pedagogy | **40L** | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |
| Examination type (SEE) | Theory | | |

**Course oSbjectives:**

- To understand Implementation strategies for digital ICS from custom to semicustom Array Design.
- To know performance parameters of CMOS circuits,
- To learn Timing issues of digital system, Memory design and Programmable logic device (PLD).

**Teaching-Learning Process (General Instructions)**
These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

**Module-1**

**Implementation Strategies For Digital ICS**: Introduction, From Custom to Semicustom and Structured Array Design Approaches, Custom Circuit Design, Cell-Based Design Methodology, Standard Cell, Compiled Cells, Macrocells, Megacells and Intellectual Property, Semi-Custom Design Flow, Array-Based Implementation Approaches, Pre-diffused (or Mask-Programmable) Arrays, Pre-wired Arrays, Perspective-The Implementation Platform of the Future.

**Module-2**

**Coping With Interconnect**: Introduction, Capacitive Parasitics, Capacitance and Reliability-Cross Talk, Capacitance and Performance in CMOS, Resistive Parasitics, Resistance and Reliability-Ohmic Voltage Drop, Electromigration, Resistance and Performance-RC Delay, Inductive Parasitics, Inductance and Reliability- Voltage Drop, Inductance and Performance-Transmission Line Effects, Advanced Interconnect Techniques,Reduced- Swing Circuits, Current-Mode Transmission Techniques, Perspective: Networks-on-a-Chip.

**Module-3**

**Timing Issues In Digital Circuits**: Introduction, Timing Classification of Digital Systems, Synchronous Interconnect, Mesochronous interconnect, Plesiochronous Interconnect, Asynchronous Interconnect, Synchronous Design — An In-depth Perspective, Synchronous Timing Basics, Sources of Skew and Jitter, Clock- Distribution Techniques, Latch-Base Clocking, Self-Timed Circuit Design, Self-Timed Logic - An Asynchronous Technique, Completion-Signal Generation, Self-Timed Signaling, Practical Examples of Self- Timed Logic, Synchronizers and Arbiters, Synchronizers-Concept and Implementation, Arbiters, Clock Synthesis and Synchronization Using a Phase-Locked Loop, Basic Concept, Building Blocks of a PLL.

**Module-4**

**Designing Memory and Array Structures**: Introduction, Memory Classification, Memory Architectures and Building Blocks, The Memory Core, Read-Only Memories, Nonvolatile Read-Write Memories, Read-Write Memories (RAM), Contents-Addressable or Associative Memory (CAM), Memory Peripheral Circuitry, The Address Decoders, Sense Amplifiers, Voltage References,Drivers/Buffers, Timing and Control.

**Module-5**

**Designing Memory and Array Structures**: Memory Reliability and Yield, Signal-to-Noise Ratio, Memory yield, Power Dissipation in Memories, Sources of Power Dissipation in Memories, Partitioning of the memory, Addressing the Active Power Dissipation, Data retention dissipation, Case Studies in Memory Design: The Programmable Logic Array (PLA), A 4Mbit SRAM, A 1 Gbit NAND Flash Memory,

Perspective: Semiconductor Memory Trends and Evolutions.

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

1. Apply design automation for complex circuits using the different implementation methodology like custom versus semi-custom, hardwired versus fixed, regular array versus ad-hoc.
2. Use the approaches to minimize the impact of interconnect parasitics on performance, power dissipation and circuit reliability
3. Impose the ordering of the switching events to meet the desired timing constraints using synchronous, clocked approach.
4. Infer the reliability of the memory
5. Understand the role of peripheral circuitry such as the decoders, sense amplifiers, drivers and control circuitry in the design of reliable and fast memories

## Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

**Suggested Learning Resources:**

**Books**


1. Jan M Rabey, AnanthaChandrakasan, Borivoje Nikolic, "Digital Integrated Circuits-A Design Perspective", PHI, 2ndEdition
2. M. Smith, "Application Specific Integrated circuits", Addison Wesley, 1997
3. Wang, Wu and Wen, "VLSI Test Principles and Architectures", Morgan Kaufmann, 2006
4. H. Veendrick, "MOS ICs: From Basics to ASICs", Wiley-VCH, 1992


**Web links and Video Lectures (e-Resources):**

- . https://archive.nptel.ac.in/courses/108/106/108106158/
- https://nptel.ac.in/courses/106106130

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Using suitable tool, design and analyze the behaviour of carry-select, carry-save, carry-lookahead and Brent-kung adder.

| NANO-ELECTRONICS | | Semester | |
|---|---|---|---|
| Course Code | **MVJ22LVL232** | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | **L:T:P: 2:2:0:0** | SEE Marks | 50 |
| Total Hours of Pedagogy | **40 L** | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |
| Examination type (SEE) | Theory | | |

**Course objectives:**

- To understand Overview of Nano science and engineering.
- To learn Quantum confinement in semiconductor nanostructures.
- To analyze different fabrication process and physical process.
- To understand various types of methods of measuring properties and applications of Nanoelectronics

**Teaching-Learning Process (General Instructions)**
These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

**Module-1**

**Introduction**: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moores' law and continued miniaturization, Classification of Nanostructures,

**Electronic properties of atoms and solids:** Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices,Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems

**Module-2**

**Characterization**: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectrometry, Techniques for property Measurement: mechanical, electron, magnetic, thermal properties

**Module-3**

**Inorganic semiconductor nanostructures**: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, and electronic density of states.

**Carbon Nanostructures**: Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes.

**Module-4**

**Fabrication techniques**: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, colloidal quantum dots, self-assembly techniques.

**Module-5**

**Physical processes**: modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intra band absorption, Light emission processes, phonon bottleneck, quantum Confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

1. Know the principles behind Nanoscience engineering and Nanoelectronics.
2. Apply the knowledge to prepare and characterize nanomaterials.
3. Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.
4. Design the process flow required to fabricate state of the art transistor technology.
5. Analyze the requirements for new materials and device structure in the future.

## Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

**Suggested Learning Resources:**

**Books**


1. Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, "Nanoscale Science and Technology", John Wiley, 2007
2. Charles P Poole, Jr, Frank J Owens, "Introduction to Nanotechnology", John Wiley Copyright 2006, Reprint 2011.
3. Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, "Hand Book of

Nanoscience Engineering and Technology", CRC press, 2003.

**Web links and Video Lectures (e-Resources):**

- . https://nptel.ac.in/courses/118104008
- https://nptel.ac.in/courses/118102003

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Using suitable tool, design and analyze the behaviour of different nano-materials.
- Using suitable tool, design and analyze the behaviour of different nono-electronics circuits.

| STATIC TIMING ANALYSIS | | Semester | 2 |
|---|---|---|---|
| Course Code | MVJ22LVL233 | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | **L:T:P: 2:2:0:0** | SEE Marks | 50 |
| Total Hours of Pedagogy | **40 L** | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |
| Examination type (SEE) | Theory | | |

**Course objectives:**

- To understand the STA Environment and concepts.
- To know standard cell library with timing model and delay model.
- To study delay calculations and timing verification concepts of flip-flops

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. 2

**Module-1**

**Introduction**: Nanometer Designs, What is Static Timing Analysis? Why Static Timing Analysis?, Crosstalk and Noise, Design Flow, CMOS Digital Designs, FPGA Designs, Asynchronous Designs, STA at Different Design Phases, Limitations of Static Timing Analysis, Power Considerations, Reliability Considerations

**STA Concepts**: CMOS Logic Design, Basic MOS Structure, CMOS Logic Gate, Standard Cells, Modeling of CMOS Cells, Switching Waveform, Propagation Delay, Slew of a Waveform, Skew between Signals, Timing Arcs and Unateness, Min and Max Timing Paths, Clock Domains, Operating Conditions

**Module-2**

**Standard Cell Library**: Pin Capacitance, Timing Modeling, Linear Timing Model, Non-Linear Delay Model, Example of Non-Linear, Delay Model Lookup, Threshold Specifications and Slew Derating Timing Models - Combinational Cells, Delay and Slew Models, Positive or Negative Unate, General Combinational Block, Timing Models - Sequential Cells, Synchronous Checks: Setup and Hold, Example of Setupand Hold Checks, Negative Values in Setup and Hold Checks, Asynchronous Checks, Recovery and Removal Checks Pulse Width Checks, Example of Recovery, Removal and Pulse Width Checks, Propagation Delay, State-Dependent Models XOR,XNOR and Sequential Cells, Interface Timing Model for a Black Box, Advanced Timing Modeling, Receiver Pin Capacitance, Specifying Capacitance at the Pin Level, Specifying Capacitance at the Timing Arc Level, Output Current, Models for Crosstalk Noise Analysis, DC Current, Output Voltage, Propagated Noise, Noise Models for Two-Stage Cells, Noise Models for Multi-stage and sequential Cells, Other Noise Models, Power Dissipation Modeling, Active Power

**Module-3**

**Interconnect Parasitics**: RLC for Interconnect, Wireload Models, Interconnect Trees, Specifying Wire load Models, Representation of Extracted Parasitic, Detailed Standard Parasitic Format ,Reduced Standard Parasitic Format, Standard Parasitic Exchange Format, Representing Coupling Capacitances, Hierarchical Methodology, Block Replicated in Layout, Reducing Parasitic for Critical Nets, Reducing Interconnect Resistance, Increasing Wire Spacing, Parasitics for Correlated Nets.

**Delay Calculation**: Overview, Delay Calculation Basics, Delay Calculation with Interconnect, Pre-layout Timing, Post-layout Timing, Cell Delay using Effective Capacitance, Interconnect Delay, Elmore Delay, Higher Order Interconnect Delay Estimation, Full Chip Delay Calculation, Slew Merging, Different Slew Thresholds, Different Voltage Domains, Path Delay Calculation, Combinational Path Delay, Path to a Flip-flop, Input to Flip-flop Path, Flip-flop to Flip-flop Path, Multiple Paths, Slack Calculation.

| Module-4 |
| --- |
| **Configuring the STA Environment**: What is the STA Environment?<br><br>Specifying Clocks, Clock Uncertainty, Clock Latency, Generated Clocks, Example of Master Clock at Clock Gating Cell Output, Generated Clock using Edge and Edge shift Options, Generated Clock using Invert Option, Clock Latency for Generated Clocks, Typical Clock Generation Scenario, Constraining Input Paths, Constraining Output Paths, Example A, Example B, Example Timing Path Groups, Modeling of External Attributes,Modeling Drive Strengths, Modeling Capacitive Load, Design Rule Checks, Virtual Clocks |
| **Module-5** |
| **Timing Verification**: Setup Timing Check, Flip-flop to Flip-flop Path, Input to Flip-flop Path, Input Path with Actual Clock, Flip flop to Output Path, Input to Output Path, Frequency Histogram, Hold Timing Check, Flip-flop to Flip- flop Path, Hold Slack Calculation, Input to Flip-flop Path, Flip-flop to Output Path, Flip-flop to Output Path with Actual Clock, Input to Output Path, Multicycle Paths, Crossing Clock Domains, False Paths, Half- Cycle Paths, Removal Timing Check, Recovery Timing Check, Timing across Clock Domains, Slow to Fast Clock Domains, Fast to Slow Clock Domains, Half-cycle Path - Case 1, Half-cycle Path -Case 2, Fast to Slow Clock Domain, Slow to Fast Clock |
| **Course outcome (Course Skill Set)**<br><br>At the end of the course, the student will be able to :<br>1. Evaluate the delay of any given digital circuits.<br>2. Prepare the resources to perform the static timing analysis using EDA tool.<br>3. Prepare timing constraints for the design based on the specification.<br>4. Generate the timing analysis report using EDA tool for different checks.<br>5. Perform verification and analyse the generated report to identify critical issues and bottleneck for the violation and suggest the techniques to make the design to meet timing |

## Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
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- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

**Suggested Learning Resources:**

**Books**


1. Bhasker, R Chadha, "Static Timing Analysis for Nanometer Designs: A Practical Approach", Springer 2009 Reference Books
2. Sridhar Gangadharan, Sanjay Churiwala, "Constraining Designs for Synthesis and Timing Analysis – A Practical Guide to Synopsis Design Constraints (SDC)", Springer, 2013
3. Naresh Maheshwari and SachinSapatnekar, "Timing Analysis and Optimization of Sequential Circuits", Springer Science and Business Media, 1999


**Web links and Video Lectures (e-Resources):**

- . https://nptel.ac.in/courses/117106149
- https://onlinecourses.nptel.ac.in/noc22_hs126/preview

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Verilog/SystemVerilog program to find the timing violations of a digital circuit.
- Verilog/SystemVerilog program to find the crosstalk/noise of a digital circuit.

| LOW POWER VLSI DESIGN | | Semester | 2 |
|---|---|---|---|
| Course Code | MVJ22LVL241 | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | **L:T:P: 2:2:0:0** | SEE Marks | 50 |
| Total Hours of Pedagogy | **40 L** | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |
| Examination type (SEE) | Theory | | |

**Course objectives:**

- To study State-of-the art approaches of power estimation and reduction.
- To understand power dissipation at various levels of design

**Teaching-Learning Process (General Instructions)**
These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

**Module-1**

**Introduction**: Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS leakage current, static current, basic principles of low power design, low power figure of merits.

**Simulation power analysis**: SPICE circuit simulation, Monte Carlo simulation.

**Module-2**

**Circuit**: Transistor and gate sizing, equivalent pin ordering, network restructuring and reorganization, special latches and flip flops, low power digital cell library, adjustable device threshold voltage.

**Module-3**

**Logic:** Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

**Low power Clock Distribution:** Power dissipation in clock distribution, single driver Vs distributed buffers.

**Module-4**

**Low power Architecture & Systems**: Power & performance management, switching activity reduction, flow graph transformation.

**Low power memory design**: Introduction, sources and reductions of power dissipation in memory subsystem.

**Module-5**

**Algorithm & Architectural Level Methodologies**: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

**Advanced Techniques**: Adiabatic computation, Asynchronous circuits.

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

1. Identify the sources of power dissipation in CMOS circuits.
2. Perform power analysis using simulation-based approaches and probabilistic analysis.
3. Use optimization and trade-off techniques that involve power dissipation of digital circuits.
4. Make the power design a reality by making power dimension an integral part of the design process.
5. Use practical low power design techniques and their analysis at various levels of design abstraction and analyse how these are being captured in the latest design automation environments.

## Assessment Details (both CIE and SEE)

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**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

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**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

**Suggested Learning Resources:**

**Books**


1. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, Kluwer Academic, 1998.
2. Jan M. Rabaey, Massoud Pedram, “Low Power Design Methodologies”, Kluwer Academic, 2010.
3. Kaushik Roy, Sharat Prasad, “Low-Power CMOS VLSI Circuit Design” Wiley, 2000
4. P. Chandrasekaran and R. W. Broadersen, “Low power digital CMOS design”, Kluwer Academic,1995.
5. A Bellamour and M I Elmasri, “Low power VLSI CMOS circuit design”, Kluwer Academic,1995.


**Web links and Video Lectures (e-Resources):**

- https://archive.nptel.ac.in/course.
- https://www.digimat.in/nptel/courses/video/106101060/L01.html

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Analyze power consumption of a circuit using SPICE simulation
- Analyze the power dissipation in memory sub-system

| SoC DESIGN | | Semester | 2 |
|---|---|---|---|
| Course Code | MVJ22LVL242 | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | **L:T:P: 2:2:0:0** | SEE Marks | 50 |
| Total Hours of Pedagogy | **40 L** | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |
| Examination type (SEE) | Theory | | |

**Course objectives:**

- To Describe the organization and implementation of the 3- and 5-stage pipeline ARM processor cores
- To Understand the needs high-level language (in this case, C) in application development
- To Know the issues involved in debugging systems in embedded processor cores and in the production testing of board-level systems.
- To learn different ARM integer cores, concept of memory hierarchy and management
- To Describe the organization and implementation of the 3- and 5-stage pipeline ARM processor cores

**Teaching-Learning Process (General Instructions)**
These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

**Module-1**

**ARM Organization and Implementation**: 3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution, ARM implementation, The ARM coprocessor interface.

**The ARM Instruction Set**: Introduction, Exceptions, Conditional execution, Branch and Branch with Link (B, BL), Branch, Branch with Link and exchange (BX, BLX), Software Interrupt (SWI).

**Module-2**

**The ARM Instruction Set** (Continued ) Data processing instructions, Multiply instructions, Count leading zeros (CLZ - architecture v5T only), Single word and unsigned byte data transfer instruction, Half-word and signed byte data transfer instructions, Multiple register transfer instructions, Swap memory and register instructions (SWP), Status register to general register transfer instructions, General register to status register transfer instructions, Coprocessor instructions, Coprocessor data operations, Coprocessor data transfers, Coprocessor register transfers, Breakpoint instruction (BRK - architecture v5T only), Unused instruction space, Memory faults, ARM architecture

**Module-3**

**Architectural Support for High-Level Languages**: Abstraction in software design, Data types, Floating-point data types, The ARM floating-point architecture, Expressions, Conditional statements ,Loops, Functions and procedures, Use of memory, Run-time environment.

**Module-4**

**Architectural Support for System Development**: The ARM memory interface, The Advanced Microcontroller Bus Architecture(AMBA), The ARM reference peripheral specification, Hardware system prototyping tools, The ARMulator, The JTAG boundary scan test architecture, The ARM debug architecture, Embedded Trace, Signal processing support

**Module-5**

**ARM Processor Cores**: ARM7TDMI, ARM8, ARM9TDMI, ARM10TDMI, Discussion, Example and exercises. **Memory Hierarchy**: Memory size and speed, On-chip memory, Caches, Cache design - an example, Memory management, Examples and exercises

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

1. Apply the 3- and 5-stage pipeline ARM processor cores and analyse the implementation iss
2. Use the concepts and methodologies employed in designing a System- on-chip (SoC) based around a microprocessor core and in designing the microprocessor core itself.
3. Understand how SoCs and microprocessors are designed and used, and why a modern processor is designed the way that it is.
4. Use integrated ARM CPU cores (including Strong ARM) that incorporate full support for memory management.
5. Analyze the requirements of a modern operating system and use the ARM architecture to address the same

## Assessment Details (both CIE and SEE)

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**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

**Suggested Learning Resources:**

**Books**


1. Steve Furber "ARM System-On-Chip Architecture" Addison Wesley, 2ndedition
2. Joseph Yiu "The Definitive Guide to the ARM Cortex-M3", Newnes, (Elsevier) , 2nd edition, 2010.
3. Sudeep Pasricha and Nikil Dutt," On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers, 2008.
4. Michael Keating, Pierre Bricaud "Reuse Methodology Manual for System on Chip designs", Kluwer Academic Publishers, 2ndedition, 2008.


**Web links and Video Lectures (e-Resources):**

- https://archive.nptel.ac.in/courses/106/106/106106134/.
- https://archive.nptel.ac.in/courses/106/105/106105193/

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Design and analyze Advanced Microcontroller Bus Architecture (AMBA)
- The JTAG boundary scan test architecture for SoC,

| SYSTEM VERILOG | | Semester | 2 |
|---|---|---|---|
| Course Code | MVJ22LVL243 | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | **L:T:P: 2:2:0:0** | SEE Marks | 50 |
| Total Hours of Pedagogy | **40 L** | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |
| Examination type (SEE) | Theory | | |

**Course objectives:**

- To understand the concepts of Verification process.
- To know the concepts of System Verilog.
- To gain the essential knowledge to write the Verification Code.
- To learn Randomization of system Verilog.
- To examine functional coverage depending upon data sample.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

**2.** .

**Module-1**

**Verification Guidelines:** The verification process, basic test bench functionality, directed testing, methodology basics, constrained random stimulus, randomization, functional coverage, test bench components, layered testbench.

**Module-2**

**Data Types:** Built in Data types, fixed and dynamic arrays, Queues, associative arrays, linked lists, array methods, choosing a storage type, creating new types with typedef, creating user defined structures, typeconversion, Enumerated types, constants and strings, Expression width

**Module-3**

**Connecting the test bench and design:** Separating the test bench and design, The interface construct, Stimulus timing, Interface driving and sampling, System Verilog assertions.

**Module-4**

**Randomization:** Introduction, Randomization in System Verilog, Constraint details, Solution probabilities, Valid constraints, Inline constraints, Random number functions, Common randomization problems

**Module-5**

**Functional Coverage:** Coverage types, Coverage strategies, Simple coverage example, Anatomy of Cover group and Triggering a Cover group, Data sampling, Cross coverage, Generic Cover groups, Coverage options, Analyzing coverage data, measuring coverage statistics during simulation.

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

1. Apply the System Verilog concepts to verify the design.
2. Understand the datatypes of System Verilog
3. Apply constrained random tests benches using System Verilog.
4. Understand Randomization
5. Appreciate Functional Coverage.

## Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

**Suggested Learning Resources:**

**Books**


1. Chris Spear, "System Verilog for Verification – A guide to learning the Test bench language features", Springer Publications Second Edition, 2010.
2. Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for Design- A guide to using system Verilog for Hardware design and modelling", Springer Publications Second Edition, 2006.


**Web links and Video Lectures (e-Resources):**

- . https://archive.nptel.ac.in/course.html
- https://nptel.ac.in/courses/106105182

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- 

| VLSI Design Lab-II | | Semester | |
|---|---|---|---|
| Course Code | **MVJ22LVLL26** | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | **L: T:P:S: 1:0:2:0** | SEE Marks | 50 |
| Credits | 02 | Exam Hours | 100 |
| Examination type (SEE) | Practical | | |

**Course objectives:**

- . Understand the features of CAD tool in VLSI design.
- Design and verify the behavior of digital circuits using digital flow
- Synthesize the circuit in VLSI tool
- Verify the design using a logic analyzer
- Analyse physical design

**Experiments to be conducted using suitable CAD tool**

| Sl.NO | Experiments |
|---|---|
| 1 | Design an Inverter with given specifications*, completing the design flow mentioned below:<br>a. Draw the schematic and verify the following<br>i) DC Analysis<br>ii) Transient Analysis<br>b. Draw the Layout and verify the DRC, ERC<br>c. Check for XX<br>d. Extract RC and back annotate the same and verify the Design<br>Verify & Optimize for Time, Power and Area to the given constraint*** |
| 2 | Design the following circuits with given specifications*, completing the design flow mentioned below:<br>a. Draw the schematic and verify the following<br>i) DC Analysis<br>ii) AC Analysis<br>iii) Transient Analysis<br>b. Draw the Layout and verify the DRC, ERC, LVS<br>c. Check for XX<br>d. Extract RC and back annotate the same and verify the Design<br>i) Single Stage differential amplifier<br>ii) Common source amplifier<br>iii) Design an op-amp with given specification* using differential amplifier<br>Commonsource amplifier in library**<br>Design a 4 bit R-2R based DAC for the given specification** |
| 3 | Design an Integrator using OPAMP (First Order) |
| 4 | Design a Differentiator using OPAMP (First Order) |
| 5 | Design and characterize a basic Sigma delta ADC from the available designs. |
| | (Any other experiments may be added in supportive of the course)<br>*Appropriate specification should be given.<br>** Applicable Library should be added & information should be given to the Designer.<br>*** An appropriate constraint should be given |

**Course outcomes (Course Skill Set):**

At the end of the course the student will be able to:

- Understand the features of CAD tool in VLSI design.
- Design and verify the behavior of digital circuits using digital flow
- Synthesize the circuit in VLSI tool
- Verify the design using a logic analyzer
- Analyse physical design

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation (CIE):**

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.

**Semester End Evaluation (SEE):**

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

**Suggested Learning Resources:**

-

| CAD OF DIGITAL SYSTEMS | | Semester | 3 |
|---|---|---|---|
| Course Code | MVJ22LVL31 | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | **L: T:P:S: 3:2:0:0** | SEE Marks | 50 |
| Total Hours of Pedagogy | **50L** | Total Marks | 100 |
| Credits | **4** | Exam Hours | 3 |
| Examination type (SEE) | Theory | | |

- To understand the basic physics and operation of MOS devices.
- To study Single-Stage and Differential Amplifiers.
- To learn Data Converter Specifications and Architectures.
- To understand Single ended Differential Amplifier and operations.
- To learn architecture of Data converter includes ADC (Analog to Digital) and DAC(Digital to Analog) Converters.

**Teaching-Learning Process (General Instructions)**
These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

**Module-1**

**Introduction to Design Methodologies**: The VLSI Design Problem, The Design Domains, Design Actions, DesignMethods and Technologies.

**VLSI Design Automation tools**: Algorithmic and System Design, Structural and Logic Design, Transistor-levelDesign, Layout Design, Verification Methods.

**Algorithmic graph theory and computational complexity**: Terminology, Data Structures for the Representation ofGraphs, Computational Complexity, Examples of Graph Algorithms.

**Tractable and intractable problems**: Decision Problems, Complexity Classes, NP-completeness and NP-hardness,

**Module-2**

**Placement and partitioning**: Circuit Representation, Wire-length Estimation, Types of Placement Problem, Placement Algorithm, Partitioning.

**Module-3**

**Routing**: Types of Local Routing Problems, Area Routing, Channel Routing, Introduction to Global Routing, Algorithms for Global Routing.

**Simulation**: General Remarks on VlSl Simulation, Gate-level Modeling and Simulation, Switch-level Modeling andSimulation.

**Module-4**

**Differential Amplifiers**: Single ended and differential operation, Basic differential pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

**Module-5**

**Data Converter Architectures**: DAC & ADC Specifications, Current Steering DAC, Charge Scaling DAC, Flash ADC, Successive Approximation ADC.

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

1. Use efficient analytical tools for quantifying the behavior of basic circuits by inspection.
2. Design high-performance, amplifier circuits with the trade-offs between speed, precision and power dissipation.
3. Design and study the behavior of phase-locked-loops for the applications.
4. Identify the critical parameters that affect the analog and mixed-signal VLSI circuits' performance
5. Perform calculations in the digital or discrete time domain, more sophisticated data converters to translate the digital data to and from inherently analog world.

## Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

**Suggested Learning Resources:**

**Books**

1. "Behzad Razavi", Design of Analog CMOS Integrated Circuits, TMH 2007.

2. "R. Jacob Baker", CMOS Circuit Design, Layout, and Simulation, Wiley Second Edition
3. "Phillip E. Allen, Douglas R. Holberg", CMOS Analog Circuit Design Oxford University Press Second Edition.

**Web links and Video Lectures (e-Resources):**

- . https://nptel.ac.in/courses/107108011
- https://archive.nptel.ac.in/courses/106/105/106105161/

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

-

| FINFETS AND OTHER MULTI-GATE TRANSISTORS | | Semester | 3 |
|---|---|---|---|
| FinFETs and Other Multi-Gate Transistors | MVJ22LVL321 | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | **L:T:P: 3:0:0** | SEE Marks | 50 |
| Total Hours of Pedagogy | **40L** | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |
| Examination nature (SEE) | Theory | | |

**Course objectives:**

- To learn the evolution of SOI MOS transistor.
- To have an insight into thin film formation techniques and advanced gate stack deposition.
- To enable the students to analyse physics behind BSIM-CMG.
- To analyse the electrostatics of the multi-gate MOS system.
- To realise the interrelationship between the multi-gate FET device properties and digital and analog circuits

**Teaching-Learning Process (General Instructions)**

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. .

**MODULE-1**

**The SOI MOSFET: From Single Gate to MultiGate**: brief history of Multiple - Gate MOSFETs, MultiGate MOSFET physics.

**MODULE-2**

**Multigate MOSFET Technology : Introduction, Active Area:Fins, Gate Stack**

**MODULE-3**

IM- CMG: A Compact Model for Mult-Gate Transistors : Introduction, Framework for MultiGate FET Modeling, MultiGate Models, BSIM-CMG and BSIM-IMG, BSIM-CMG.

**MODULE-4**

**Physics of the MultiGate MOS system** : Device electrostatics, Double gate MOS system, Two-dimensional confinement.

**MODULE-5**

Multi-Gate MOSFET circuit Design : Introduction, Digital Circuit Design, Analog Circuit Design

**Course outcomes (Course Skill Set):**
At the end of the course, the student will be able to:

- List out the advantages and challenges of Multi-gate Fin FETs.
- Describe thin film formation technique, gate stack deposition and physics beyond BSIM-CMG.
- Analyse electrostatics of multi-gate MOS system and corelate multigate FET device properties and elementary digital and analog circuits.

## Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

5. The question paper will have ten questions. Each question is set for 20 marks.
6. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
7. The students have to answer 5 full questions, selecting one full question from each module.
    - Marks scored shall be proportionally reduced to 50 marks

**Suggested Learning Resources:**

**Books**


1. J.P.Colinge,: FinFETs and other Multi-Gate Transistors, springer, Series on Integrated Circuits and Systems.
2. Samar Saha, : Fin FET Devices for VLSI Circuits and Systems, CRC Press, First Edition, 2020
3. Weihua Han,Zhiming M. Wang, : Toward Quantum FinFET , Springer Cham, First Edition 2021.

4. Yogesh singh Chauhan, Darsen D, et.al , FinFET Modeling for IC Simulation and Design: using the BSIM-CMG standard, Academic Press, 2015.

**Web links and Video Lectures (e-Resources):**

- https://archive.nptel.ac.in/courses/108/108/108108111/
- https://archive.nptel.ac.in/courses/117/107/117107149/

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

| VLSI DESIGN FOR SIGNAL PROCESSING | | Semester | 3 |
|---|---|---|---|
| Course Code | **MVJ22LVL322** | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | **L:T:P: 3:0:0** | SEE Marks | 50 |
| Total Hours of Pedagogy | **40 L** | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |
| Examination type (SEE) | Theory | | |

**Course objectives:**

- To learn the Transformations for high speed design using pipelining, retiming, and parallel processing techniques
- To understand the Power reduction transformations for supply voltage reduction as well as for strength or capacitance reduction
- To analyse area reduction using folding techniques
- To create Strategies for arithmetic implementation
- To create Strategies for arithmetic implementation

**Teaching-Learning Process (General Instructions)**
These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.
.

**Module-1**

**Introduction to DSP Systems**: Typical DSP Algorithms, DSP Application Demands and Scaled CMOS Technologies, Representations of DSP Algorithms.

**Iteration Bounds**: Data flow graph Representations, loop bound and Iteration bound. Algorithms for ComputingIteration Bound, Iteration Bound of multi rate data flow graphs.

**Module-2**

**Pipelining and Parallel Processing**: pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power.

**Retiming**: Definition and Properties, Solving Systems of Inequalities, Retiming Techniques.

**Module-3**

**Unfolding**: An Algorithm for Unfolding, Properties of Unfolding, Critical path, Unfolding and Retiming, Application of Unfolding.

**Folding**: Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding of Multirate Systems.

**Module-4**

**Systolic Architecture Design**: systolic array design Methodology, FIR systolic array, Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D systolic Array Design, Systolic Design forspace representation containing Delays.

**Fast convolution**: Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution, cyclic convolution Design of fast convolution Algorithm by Inspection.

**Module-5**

**Pipelined and Parallel Recursive and Adaptive Filter**: Pipeline Interleaving in Digital Filter, first order IIR digital Filter, Higher order IIR digital Filter, parallel processing for IIR filter, Combined pipelining and parallel processing for IIR Filter, Low power IIR Filter Design Using Pipelining and parallel processing, pipelined adaptive digital filter.

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

1. Illustrate the use of various DSP algorithms and addresses their representation using block diagrams, signal flow graphs and data-flow graphs
2. Use pipelining and parallel processing in design of high-speed /low-power
3. applications
4. Apply unfolding in the design of parallel architecture.
5. Evaluate the use of look-ahead techniques in parallel and pipelined IIR Digital filters.
6. Develop an algorithm or architecture or circuit design for DSP applications

## Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

8. The question paper will have ten questions. Each question is set for 20 marks.
9. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
10. The students have to answer 5 full questions, selecting one full question from each module.
11. Marks scored shall be proportionally reduced to 50 marks

**Suggested Learning Resources:**

**Books**


1. Keshab K.Parthi , VLSI Digital Signal Processing systems, Design and implementation, Wiley, 1999
2. Mohammed Isamail and Terri Fiez , Analog VLSI Signal and Information Processing, Mc Graw-Hill, 1994
3. S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985
4. Jose E. France, Yannis Tsividis, Design of Analog - Digital VLSI Circuits forTelecommunication and Signal Processing. Prentice Hall, 1994
5. Lars Wanhammar, DSP Integrated Circuits, Academic Press Series in Engineering, 1stEdition


**Web links and Video Lectures (e-Resources):**

- . https://archive.nptel.ac.in/courses/106/102/106102163/

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

-

| ADVANCES IN IMAGE PROCESSING | | Semester | 3 |
|---|---|---|---|
| Course Code | **MVJ22LVL323** | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | **L:T:P: 3:0:0** | SEE Marks | 50 |
| Total Hours of Pedagogy | **40 L** | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |
| Examination type (SEE) | Theory | | |

**Course objectives:**

- Understand the representation of the digital image and its properties.
- Apply pre-processing techniques required to enhance the image for its further analysis.
- Use segmentation techniques to select the region of interest in the image for analysis.
- Represent the image based on its shape and edge information and also describe the objects present in theimage based on its properties and structure.
- Use morphological operations to simplify images, and quantify and preserve the main shape characteristic of the objects.

**Teaching-Learning Process (General Instructions)**
These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.
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**Module-1**

The image, its representations and properties: Image representations a few concepts, Image digitization, Digitalimage properties, Color images.

**Module-2**

Image Pre-processing: Pixel brightness transformations, geometric transformations, local pre-processing.

**Module-3**

Segmentation: Thresholding; Edge-based segmentation – Edge image thresholding, Edge relaxation, Border tracing, Hough transforms; Region – based segmentation – Region merging, Region splitting, Splitting and merging, Watershed segmentation, Region growing post-processing.

**MODULE 4**

Shape representation and description: Region identification; Contour-based shape representation anddescription – Chain codes, Simple geometric border representation, Fourier transforms of boundaries,

Boundary description using

segment sequences, B-spline representation; Region-based shape representation and description – Simple scalarregion descriptors, Moments, Convex hull.

**Module-5**

Mathematical Morphology: Basic morphological concepts, Four morphological principles, Binary dilation anderosion, Skeletons and object marking, Morphological segmentations and watersheds.

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

- Understand the representation of the digital image and its properties.
- Apply pre-processing techniques required to enhance the image for its further analysis.
- Use segmentation techniques to select the region of interest in the image for analysis.
- Represent the image based on its shape and edge information and also describe the objects present in the image based on its properties and structure.
- Use morphological operations to simplify images, and quantify and preserve the main shape characteristics of the objects

## Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

12. The question paper will have ten questions. Each question is set for 20 marks.
13. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
14. The students have to answer 5 full questions, selecting one full question from each module.
15. Marks scored shall be proportionally reduced to 50 marks

**Suggested Learning Resources:**

**Books**


6. Keshab K.Parthi , VLSI Digital Signal Processing systems, Design and implementation, Wiley, 1999
7. Mohammed Isamail and Terri Fiez , Analog VLSI Signal and Information Processing, Mc Graw-Hill, 1994
8. S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985
9. Jose E. France, Yannis Tsividis, Design of Analog - Digital VLSI Circuits forTelecommunication and Signal Processing. Prentice Hall, 1994
10. Lars Wanhammar, DSP Integrated Circuits, Academic Press Series in Engineering, 1stEdition


**Web links and Video Lectures (e-Resources):**

- . https://archive.nptel.ac.in/courses/106/102/106102163/

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- 

| RECONFIGURABLE COMPUTING | | Semester | 3 |
|---|---|---|---|
| Course Code | MVJ22LVL331 | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | **L:T:P: 3:0:0** | SEE Marks | 50 |
| Total Hours of Pedagogy | **40 L** | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |
| Examination type (SEE) | Theory | | |

**Course objectives:**

- To understand the Reconfigurable vs Processor based system, RC Architecture
- To know Partial Reconfiguration Design
- To study Reconfigurable computing for DSP

**Teaching-Learning Process (General Instructions)**
These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

**2.** .

**Module-1**

**Introduction**: History, Reconfigurable vs Processor based system, RC Architecture.

**Reconfigurable Logic Devices**: Field Programmable Gate Array, Coarse Grained ReconfigurableArrays. **Reconfigurable Computing System**: Parallel Processing on Reconfigurable Computers, A survey ofReconfigurable Computing System. (Text 1)

**Module-2**

**Languages and Compilation**: Design Cycle, Languages, HDL, High Level Compilation, Low level Design flow,

Debugging Reconfigurable Computing Applications. (Text 1)

**Module-3**

**Implementation**: Integration, FPGA Design flow, Logic Synthesis.

**High Level Synthesis for Reconfigurable Devices:** Modelling, Temporal Partitioning Algorithms. (Text 2)

**Module-4**

**Partial Reconfiguration Design**: Partial Reconfiguration Design, Bitstream Manipulation with JBits, Themodular Design flow, The Early Access Design Flow, Creating Partially Reconfigurable Designs, Partial

Reconfiguration using Hansel-C Designs, Platform Design. (Text 2)

**Module-5**

**Signal Processing Applications**: Reconfigurable computing for DSP, DSP application building blocks, Examples: Beamforming, Software Radio, Image and video processing, Local Neighbourhood functions, Convolution. (Text 1)

**System on a Programmable Chip**: Introduction to SoPC, Adaptive Multiprocessing on Chip.(Text 2)

**Course outcomes:**

At the end of the course the student will be able to:

1. Understand the fundamental principles and practices in reconfigurable architecture.
2. Simulate and synthesize the reconfigurable computing architectures.
3. Understand the FPGA design principles, and logic synthesis
4. Integrate hardware and software technologies for reconfiguration computing focusing on partial reconfiguration design.
5. Design digital systems for a variety of applications on signal processing and system on chip

configurations

## Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

**Suggested Learning Resources:**

**Books**


1. Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays M. Gokhale and P.Graham Springer, ISBN: 978-0-387-26105-8 2005

2. Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications C. Bobda Springer,

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|---|
| ISBN: 978-1-4020-6088-5 2007 |
| **Web links and Video Lectures (e-Resources):** |
| • . https://archive.nptel.ac.in/courses/106/105/106105196/ |
| **Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**<br>• |

| LONG TERM RELIABILITY OF VLSI SYSTEMS | | Semester | 3 |
|---|---|---|---|
| Course Code | **MVJ22LVL332** | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | **L:T:P: 3:0:0** | SEE Marks | 50 |
| Total Hours of Pedagogy | **40 L** | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |
| Examination type (SEE) | Theory | | |

**Course objectives:**

- To understand Overview of Nano science and engineering.
- To learn Quantum confinement in semiconductor nanostructures.
- To analyze different fabrication process and physical process.
- To understand various types of methods of measuring properties and applications of Nanoelectronics

**Teaching-Learning Process (General Instructions)**
These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

**3.** .

**Module-1**

**Electromigration Reliability**

Why Electromigration Reliability?,Why system-level EM Reliability Management? Physics- based EM Modeling, Electromigration Fundamentals, Stress based EM Modeling and stress diffusion equations, Modeling for transient EM effects and Initial stress conditions, post voiding stress and void volume evolution, compact physics based EM model for a single wire, other relevant EM models and analysis methods. (Text Book:1 – 1.1, 1.2, 2.1 up to 2.6, 2.9).

**Module-2**

**Fast EM Stress Evolution Analysis**

Introduction, The LTI ordinary differential equations for EM stress evolution, The presented Krylov fast EM stress analysis, Numerical results and discussions (Text. Book:1 – 3.1 up to 3.4).

**Module-3**

**EM Assessment for Power Grid Networks**

New power grid reliability analysis method, cross-layout temperature and thermal stress characterization, impact of across-layout temperature and thermal stress on EM. (Text.Book:1 – 7.1, 7.2, 7.4, 7.5).

**Module-4**

**Transistor Aging Effects and Reliability:**

Introduction, Transistor reliability in advanced technology nodes, Transistor Aging, BTI- Bias Temperature Instability, HCI – Hot Carrier Injection, Coupling models for BTI and HCI degradations, RTN – Random Telegraph Noise, TDDB – Time Dependent Dielectric Breakdown. (Text Book: 1 – 13.1, 13.2).

**Module-5**

**Aging Effects in Sequential Elements:**

Introduction, Background: flip flop timing analysis, process variation model, voltage droop model,

Robustness analysis, reliability-aware flip-flop design (Text Book: 1 – 16.1 up to 16.4).

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

1. Comprehend the recent research in the area of interconnect and device reliability.
2. Determine the impact of device-level reliability on system performance, built upon physics-basedmodels.
3. Understand the physics-based EM modeling.
4. Understand the underlying phenomena of BTI, HCI, TDDB leading to device-level reliability degradation.
5. Relate to considerations at the circuit-level with both combinational and sequential elements

## Assessment Details (both CIE and SEE)

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2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

**Suggested Learning Resources:**

**Books**

1. Long-Term Reliability of Nanometer VLSI Systems Sheldon X. D. Tan, Mehdi Springer International 1st Edition, 2019 BaradaranTahoori, Publishing ISBN: 978-3- Taeyoung Kim, 030-26171-9

**Web links and Video Lectures (e-Resources):**

- . https://archive.nptel.ac.in/courses/108/107/108107113/

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

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| CMOS RF Circuit Design | | Semester | 3 |
|---|---|---|---|
| Course Code | MVJ22LVL333 | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | **L:T:P: 3:0:0:0** | SEE Marks | 50 |
| Total Hours of Pedagogy | **40 L** | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 hrs |
| Examination type (SEE) | Theory | | |

**Course objectives:**

- To study State-of-the art approaches of power estimation and reduction.
- To understand power dissipation at various levels of design

**Teaching-Learning Process (General Instructions)**
These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

**Module-1**

**Introduction to RF Design, Wireless Technology and Basic Concepts**: A wireless world, RF design is challenging, The big picture. General considerations, Effects of Nonlinearity, Noise, Sensitivity and dynamic range, Passive impedance transformation. Scattering parameters, Analysis of nonlinear dynamic systems,

conversion of gains and distortion

**Module-2**

**Communication Concepts**: General concepts, analog modulation, digital modulation, spectral re-growth,coherent and non-coherent detection, Mobile RF communications, Multiple access techniques, Wireless

standards, Appendix 1: Differential phase shift keying.

**Module-3**

**Transceiver Architecture**: General considerations, Receiver architecture, Transmitter architectures, Direct conversion and two-step transmitters, RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub

sampled receivers.

**Module-4**

**Low Noise Amplifiers and Mixers**: General considerations, Problem of input matching, LNAtopologies: common-source stage with inductive load, common-source stage with resistive feedback.

Mixers-General considerations, passive down conversion mixers, Various mixers- working and implementation.

**Module-5**

**VCO and PLLs**- Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off.

Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS,Various RF synthesizer architectures and frequency dividers, Power Amplifier design.

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

1. Identify the sources of power dissipation in CMOS circuits.
2. Perform power analysis using simulation-based approaches and probabilistic analysis.
3. Use optimization and trade-off techniques that involve power dissipation of digital circuits.
4. Make the power design a reality by making power dimension an integral part of the design process.
5. Use practical low power design techniques and their analysis at various levels of design abstraction and analyse how these are being captured in the latest design automation environments.

## Assessment Details (both CIE and SEE)

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3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

**Suggested Learning Resources:**

**Books**

1. RF Microelectronics B. Razavi PHI second edition
2. CMOS Circuit Design, layout and Simulation R. Jacob Baker, H.W. Li, D.E. Boyce PHI 1998

**Web links and Video Lectures (e-Resources):**

- . https://archive.nptel.ac.in/courses/117/102/117102012/

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

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