B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: III		
ANALOG ELECTRONICS		
Course Code:	**MVJ22VL32**	**CIE Marks:100**
Credits:	**L:T:P: 3:0:2**	**SEE Marks: 100**
Hours:	**40L+26P**	**SEE Duration: 3 Hrs**

Course Learning Objectives: The students will be able to	
1	Understand low frequency response for various configurations of BJT and FET amplifier.
2	Understand the different topologies of feedback amplifiers and oscillators.
3	Compare various types of DACs and ADCs, timer IC's and evaluate the performance of each with neat circuit diagrams.
4	Analyze typical frequency response graphs for each of the filter circuits and switching circuits of Op-Amps.
5	Analyze different oscillator, filters, rectifiers and transistor configurations.

UNIT 1	
P-N Junction Diode: Load line analysis, diode applications - Limiters, clippers, clampers, voltage multipliers, half wave & full wave rectification. **Special Purpose Diodes** - Zener diode, varactor diode, light emitting diodes, laser diodes. **Laboratory Sessions/ Experimental Learning:** 1. Construct and analyze a full-wave rectifier **Applications:** Half wave and full wave rectifiers, clippers and clampers	**8Hrs.**
UNIT 2	
Bipolar Junction Transistors (BJT): Introduction, DC operating point, fixed bias, emitter bias with and without emitter resistance, voltage divider bias, dc bias with voltage feedback, analysis of above circuits and their design, variation of operating point and its stability. **Laboratory Sessions/ Experimental Learning:** 1. Plot the transfer and drain characteristics of a BJT and calculate its drain resistance, mutual conductance and amplification factor. **Applications:** Small signal amplifiers, oscillators, voltage regulators, sensors	**8Hrs.**
UNIT 3	

Transistors Amplifier: Small signal BJT amplifiers: AC equivalent circuit, hybrid, re model and their use in amplifier design. Multistage amplifiers, frequency response of basic & compound configuration. **Laboratory Sessions/ Experimental Learning:** 1. Plot the frequency response using any class of power amplifier. **Applications:** Power amplifiers	**8Hrs.**
UNIT 4	
OP-Amps and its Applications: Ideal Op-Amp, practical op-amp circuits, differential and common mode operation, inverting & non inverting amplifier, integrator, differentiator, summing, scaling and averaging amplifiers, buffer, instrumentation amplifier, Schmitt Trigger **Active Filters**: First and second order low-pass and high-pass Butterworth filters, band-pass filters, band reject filters. **Laboratory Sessions/ Experimental Learning:** 1. Design and test the voltage-shunt feedback amplifier and calculate the parameters using with and without feedback. 2. Design and find the gain of a differential amplifier. **Applications:** Amplifiers, filters, oscillators, comparators	**8Hrs.**
UNIT 5	
Feedback Circuits: Effect of positive and negative feedbacks, basic feedback topologies & their properties, Analysis of practical feedback amplifiers. **Oscillators:** Oscillator operation, FET based phase shift oscillator, Wien bridge oscillator, LC and crystal oscillators. **555 Timer and its Applications:** Mono-stable and astable multivibrators. **Laboratory Sessions/ Experimental Learning:** 1. Construct a Wien Bridge Oscillator circuit using an operational amplifier and analyse the output waveform. **Applications:** Waveform generation, servo-system	**8Hrs.**

Course Outcomes: After completing the course, the students will be able to	
CO1	Explain the principles of analog electronic circuits, describing device characteristics such as transistor operation modes, biasing techniques, and small-signal models.
CO2	Apply knowledge of analog circuit analysis to design and simulate basic amplifier circuits, filters, and oscillators.
CO3	Analyze the performance of analog circuits by evaluating frequency response, gain-bandwidth product, and stability criteria.
CO4	Design analog integrated circuits (ICs) by integrating transistor-level designs into functional blocks such as operational amplifiers (op-amps).
CO5	Design, test and utilize various types of op amps for many applications

LIST OF EXPERIMENTS

S. No.	Experiment Name
1	Design a monostable multivibrator using 555 timer.
2	Design a astable multivibrator using 555 timer.
3	Design a RC phase shift oscillator.
4	Design a inverting Schmitt trigger.
5	Design a narrow band-pass filter and narrow band-reject filter.
6	Design a precision full-wave rectifier.
7	Input and output characteristics of transistor CB configuration
8	Input and output characteristics of transistor CE configuration

Text Books	
1.	Robert L. Boylestad and Louis Nashelsky, "Electronic Devices and Circuit Theory", PHI/Pearson Education,11th Edition.
2.	Adel S Sedra, Kenneth C Smith "Microelectronic Circuits, Theory and Applications", 6th Edition, Oxford, 2015.ISBN:978-0-19-808913-1.
Reference Books	
1.	Behzad Razavi, "Fundamentals of Microelectronics", John Weily ISBN 2013 978-81-265-2307-8,2nd Edition.
2.	K.A. Navas, "Electronics Lab Manual", Volume I, PHI, 5th Edition, 2015, ISBN: 9788120351424.

3.	"Linear Integrated Circuits", D. Roy Choudhury and Shail B. Jain, 4th edition, New Age International ISBN 978-81-224-3098-1.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

Laboratory- 50 Marks

Experiment Conduction with proper results is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

CO-PO-PSO Mapping

CO/ PO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
CO1	3	3	1	2	2	-	-	-	-	-	-	2	1	1
CO2	3	3	1	3	2	-	-	-	-	-	-	2	1	1
CO3	3	3	2	3	2	-	-	-	-	-	-	2	1	1
CO4	3	3	2	2	2	-	-	-	-	-	-	2	1	1
CO5	3	3	2	2	2	-	-	1	2	-	-	2	1	1

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: III		
PHYSICS OF SEMICONDUCTOR DEVICES		
Course Code:	**MVJ22VL33**	**CIE Marks: 50**
Credits:	**L:T:P: 3:0:2**	**SEE Marks: 50**
Hours:	**40L+26P**	**SEE Duration: 3 Hrs**

Course Learning Objectives: The students will be able to	
1	Understand the fundamentals of intrinsic, extrinsic semiconductors with carrier concentration.
2	Analyze the current-voltage characteristics of a diode.
3	Analyze the performance and behavior of semiconductor devices under different operating conditions by examining capacitance-voltage (C-V) profiles.
4	Analyze various short channel effects in MOSFET.
5	Understand the basic structure and operational principles of FinFETs.

UNIT 1	
Semiconductor Fundamentals: Crystal structure, quantum mechanics, energy bands and charge carriers in solids, Fermi level, carrier concentration in semiconductors, intrinsic and extrinsic semiconductors, density of states, Fermi distribution, equilibrium concentration, Boltzmann statistics, direct and indirect band-gap. **Carrier Transport in Semiconductors:** Current flow mechanisms: Drift current, diffusion current, mobility of carriers, current density equations, continuity equation. **Laboratory Sessions/ Experimental Learning:** 1. Measure and compare the resistivity of intrinsic and extrinsic (doped) semiconductors **Applications:** Direct bandgap semiconductors are used in LED and LASER	**8Hrs.**
UNIT 2	
P-N Junction: Energy band diagrams, space charge layers, poisson equation, electric fields and potentials, p-n junction under applied bias, static current-voltage characteristics of p-n junctions, breakdown mechanisms (Avalanche breakdown, Zener process), Reverse bias junction capacitance. **Laboratory Sessions/ Experimental Learning:**	**8Hrs.**

1. Observe the current-voltage behavior of a diode in forward and reverse bias **Applications:** Transient voltage suppression (TVS) diodes	
UNIT 3	
Metal Semiconductor Contact: Ideal MS contact, ohmic contact, rectifying contact, schottky diode. **MOS Capacitor:** Ideal MOS fundamentals**,** accumulation, depletion and inversion, threshold voltage, factors affecting the threshold voltage, CV characteristics of ideal MOS. **Laboratory Sessions/ Experimental Learning:** 1. Measure the gate capacitance of MOSCAP and understand its variation with applied voltage. **Applications:** DRAM, capacitive sensors, charged coupled devices	**8Hrs.**
UNIT 4	
Non Ideal MOS: Metal semiconductor work function difference**,** oxide charges: Mobile ions, fixed charges, interfacial traps, induce charges, CV characteristics of non-ideal MOS. **MOSFETs:** Theory of operation, I_D-V_D characteristics, I_D-V_G characteristics, Scaling and Short Channel Effects, drain-induced barrier lowering, velocity saturation, impact ionization, Channel length modulation, Hot carrier effect. **Laboratory Sessions/ Experimental Learning:** 1. Measure the I_D –V_D at various gate voltage for n channel MOSFET. **Applications:** Switching devices, amplifiers, digital circuits, RF and microwave circuits	**8Hrs.**
UNIT 5	
Modern FET Structures: FinFETs, structure and design of FinFET, benefits over Planar MOSFETs, SOI (Silicon on insulator) MOSFET, GAAFETs (Gate-All-Around FETs). **Laboratory Sessions/ Experimental Learning:** 1. Measure the I-V characteristics and efficiency of a SOI MOSFET. **Applications:** Microprocessor and CPU, smartphone, tablets	**8Hrs.**

Course Outcomes: After completing the course, the students will be able to	
CO1	Explain the band structure diagrams of intrinsic and extrinsic semiconductors.
CO2	Solve the electrostatics of PN junction diode and draw its characteristics in positive and negative bias.
CO3	Analyze the fundamentals parameters of MOS capacitor.
CO4	Understand various modern FET architectures
CO5	Examine and evaluate the performance of various types of diodes and MOSFET.
LIST OF EXPERIMENTS	
S. No.	**Experiment Name**
1.	To study the I-V characteristics of a PN junction diode and understand its behaviour under forward and reverse bias conditions.
2.	Examine the operation of the Zener diode and plot its characteristic curve for both forward and reverse bias.
3,	Apply Zener diode to make stable voltage regulator(VR)
4.	To examine the I-V characteristics of an n-channel MOSFET.
5.	To understand MOS operation in different regions (cut off, linear, and saturation).
6.	To understand the transfer characteristics of (ID vs VGS) characteristics of MOS operation and analyse DIBL effect by varying VDS=0.05 and VDS=1.05
7.	To study the electrical characteristics of light emitting diodes (LEDs)
Text Books:	
1.	Semiconductor Device Fundamentals" by Robert F. Pierret, Addison-Wesley, ISBN: 0-201-54393-1
2.	Streetman, B. and Banerjee, S., Solid State Electronics, Prentice Hall India.
Reference Books:	
1.	Sze, S.M., Physics of Semiconductor Devices, John Wiley.
2.	Advanced Semiconductor Fundamentals" by Robert F. Pierret, Addison-Wesley, ISBN: 0-201-54393-1

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

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Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

Laboratory- 50 Marks

Experiment Conduction with proper results is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**1**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO2	**3**	**3**	**1**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**1**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**1**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**1**	**2**	**2**	**-**	**-**	**1**	**2**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: III		
ANALYSIS AND DESIGN OF DIGITAL CIRCUITS		
Course Code:	**MVJ22VL34**	**CIE Marks:50**
Credits:	**L:T:P:S 3:0:0:Y**	**SEE Marks: 50**
Hours:	**40 L**	**SEE Duration: 03 Hours**

Course Learning Objectives: The students will be able to	
1	Explain the basic principles of digital logic design, including the operation of logic gates, flip-flops, and the distinction between combinational and sequential circuits.
2	Interpret Boolean expressions and demonstrate the use of truth tables and Karnaugh maps in simplifying logical expressions for combinational circuits.
3	Apply digital design principles to construct basic combinational circuits.
4	Design sequential circuits, such as counters and shift registers, by utilizing flip-flops.
5	Design digital systems using programmable logic devices (PLDs).

UNIT-I	
Prerequisites: *Number systems, Boolean Algebra, Logic Gates* **Principles of Combinational Logic**: Introduction, canonical forms, generation of switching equations from truth tables, Karnaugh maps-3, 4 variables, incompletely specified functions (Don't care terms), Quine- McClusky techniques- 3 & 4 variables. **Laboratory Sessions/ Experimental Learning**: 1. Study of Logic Gates – NOT, OR, AND, NOR, NAND, XOR and XNOR. 2. Design a 4-bit Binary to Gray code converter using logic gates. **Applications:** OR gate in detecting exceed of threshold values and producing command signal for the system and AND gate in frequency measurement.	**8 Hrs**
UNIT-II	
Design and Analysis of Combinational Logic: Half adder & subtractor, full adder & subtractors, parallel adder and subtractor, look ahead carry adder, BCD adder, binary comparators, multiplexers and demultiplexers, decoders, encoders, priority encoder **Laboratory Sessions/ Experimental Learning:**	**8 Hrs**

1. Design a full adder with two half adders using logic gates. 2. Design an Adder cum Subtractor circuit which adds when input bit operation=1 or subtract if 0, using logic gates. 3. Design 4-bit comparator using IC7485. 4. Realize a Boolean expression using decoder IC74139. **Applications:** Communication systems, speed synchronization of multiple motors in industries.	
UNIT-III	
Flip-Flops and its Applications: Latches and flip flops, master-slave JK flip-flop, timing concerns in sequential circuits, shift registers – SISO, SIPO, PISO PIPO, universal shift register, counters – synchronous and asynchronous. **Laboratory Sessions/ Experimental Learning:** 1. Develop SR, D, JK &T flip flop using logic gates 2. Design a 6-bit Register using D-Flipflop **Applications:** Frequency divider circuit, frequency counter.	**8 Hrs**
UNIT-IV	
Sequential Circuit Design: Characteristic equations, design of a synchronous mod-n counter using clocked JK, D, T and SR flip-flops, Melay & Moore models, design of a sequence detector. **Laboratory Sessions/ Experimental Learning:** 1. Design a synchronous counter for a given sequence- 0, 2, 4, 6, 0 2. Design a 4-bit asynchronous up/down counter 3. Design a 4-bit binary synchronous up/down **Applications:** Data synchronizer, counter.	**8 Hrs**
UNIT-V	
Memory Devices: Basic memory structure: ROM, PROM, EPROM, EEPROM, RAM- Static and dynamic RAM Programmable Logic Devices: Programmable Logic Array (PLA), Programmable Array Logic (PAL), Field Programmable Gate Arrays (FPGA), Implementation of combinational logic circuits using PLA, PAL. **Laboratory Sessions/ Experimental Learning:**	**8 Hrs**

1. Designing of combinational logic circuits using PLA, PAL.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Describe the algebraic equations using K-map & Quine-McCluskey technique.
CO2	Explain the operation and characteristics of fundamental digital electronic components, including logic gates, flip-flops, and multiplexers, and describe their roles in digital circuits.
CO3	Interpret and construct truth tables and Boolean expressions for various digital logic circuits.
CO4	Apply digital design techniques to develop combinational and sequential circuits.
CO5	Analyze and design finite state machines (FSMs) by evaluating state transition diagrams, constructing state tables, and designing sequential circuits using FSMs.
Text Books:	
1.	Morris Mano, ―Digital Design , Prentice Hall of India, Third Edition.
Reference Books:	
1.	Charles H Roth Jr., Larry L. Kinney ―Fundamentals of Logic Design, CengageLearning 7th Edition.
2.	Donald D. Givone, "Digital Principles and Design", McGraw Hill.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

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Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20

marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: III		
DIGITAL CIRCUIT LABORATORY		
Course Code:	**MVJ22VLL35**	**CIE Marks: 50**
Credits:	**L:T:P:0:0:2**	**SEE Marks: 50**
Hours:	**26P**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Understand digital logic levels and application of knowledge to further understand digital electronics circuits.	
2	Analyze the design of various digital electronic circuits.	
3	Apply the knowledge of digital circuits and systems to efficiently, reliably, and economically to achieve desired results.	
4	Execute the techniques for modelling and troubleshooting circuits and systems through structural and gate-level networks and breadboard designs.	
5	Analyze the timing diagrams of digital circuits to understand their temporal behavior.	

LIST OF EXPERIMENTS	
S. No.	**Experiment Name**
1	To study and verify truth table of logic gates
2	To realize half/full adder and half/full subtractor
3	To realize IC7483 as parallel adder/subtractor
4	To verify BCD to excess 3-code conversion using NAND gates. To study and verify the truth table of excess-3 to BCD code convertor
5	To convert given binary numbers to gray code.
6	To verify truth table of MUX and DEMUX using NAND
7	To verify the truth table of one bit and two bit comparators using logic gates
8	To convert a given octal input to binary output and to study the LED display using 7447 7-segment decoder
9	To verify the truth table of flipflops
10	To design bi-synchronous counter using T-flipflop
Course Outcomes: After completing the course, the students will be able to	
CO1	Understand the fundamental concepts and techniques used in digital electronics.

CO2	Identify and describe the functions of various digital components.
CO3	Solve boolean functions using logic gates.
CO4	Describe the truth tables of different combinational & sequential circuits.
CO5	Analyze the performance and behavior of digital circuits.

CO-PO-PSO Mapping														
CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
CO1	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**1**	**3**	**-**	**-**	2	**1**	**1**
CO2	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**1**	**3**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**1**	**3**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**1**	**3**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**1**	**3**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: III		
PRINCIPLES OF COMMUNICATION		
Course Code:	**MVJ22VL361**	**CIE Marks:50**
Credits:	**L:T:P 3:0:0**	**SEE Marks: 50**
Hours:	**40 L**	**SEE Duration: 03 Hours**

Course Learning Objectives: The students will be able to

1	Explain the fundamental principles of analog and digital communication systems, including modulation techniques, signal transmission, and reception.
2	Apply modulation and demodulation techniques to design analog communication systems.
3	Analyze the performance of digital communication systems by evaluating parameters such as bit error rate (BER), signal-to-noise ratio (SNR), and bandwidth efficiency.
4	Implement digital modulation schemes such as pulse code modulation (PCM), and quadrature amplitude modulation (QAM).
5	Apply the basic concepts of coherent and non-coherent digital modulation techniques and understand the basics of spread spectrum modulation.

UNIT-I

Introduction: Basic block diagram of communication system, Need of Modulation, types of modulation **Amplitude Modulation:** Introduction to AM, time-domain description, frequency-domain description, single-tone modulation, generation of AM wave: Square law modulator, switching modulator, detection of AM waves: Envelope detector **Double Side Band Suppressed Carrier (DSBSC) and SSB Modulation:** Time-domain description and frequency-domain representation **Laboratory Sessions/ Experimental Learning:** 1. Generation of AM signal using MATLAB. 2. Generation of DSBSC signal using transistor. **Applications:** Broadcast transmissions, Air band radio, Quadrature amplitude modulation.	**8 Hrs**

UNIT-II

Angle Modulation: Basic concepts of Phase Modulation, Frequency Modulation: Narrow band FM, wide band FM, and generation of FM waves: Indirect FM and direct FM. Detection of FM Signal: Balanced slope detector, Phase locked loop, Comparison of FM and AM., Concept of Pre-emphasis and de-emphasis. **Laboratory Sessions/ Experimental Learning:** 1. Generation of FM signal using MATLAB **Applications:** FM radio broadcasting, telemetry, radar, seismic prospecting, and monitoring new-born for seizures via EEG, two-way radio systems, sound synthesis, magnetic tape- recording systems and some video-transmission systems.	**8 Hrs**
UNIT-III	
Transmitters: Classification of Transmitters, AM Transmitters, FM Transmitters **Receivers**: Radio Receiver - Receiver Types - Tuned radio frequency receiver, Super heterodyne receiver, RF section and Characteristics - Frequency changing and tracking, Intermediate frequency, Image frequency, AGC, Amplitude limiting, FM Receiver, Comparison of AM and FM Receivers. **Laboratory Sessions/ Experimental Learning:** 1. Investigate the effects of noise on analog modulation signals and explore noise reduction techniques. **Applications:** Biomedical engineering, communication systems	**8 Hrs**
UNIT-IV	
Pulse Modulation: Types of Pulse modulation- PAM, PWM and PPM. Comparison of FDM and TDM Pulse Code Modulation: PCM Generation and Reconstruction, Quantization Noise, Non-Uniform Quantization and Companding, DPCM, Adaptive DPCM, DM and Adaptive DM, Noise in PCM and DM. **Laboratory Sessions/ Experimental Learning:** 1. Eye diagram using MATLAB **Applications:** Ethernet, RFID marker localization signals, Radar Systems	**8 Hrs**
UNIT-V	
Digital Modulation Techniques: ASK- Modulator, Coherent ASK Detector, FSK-	**8 Hrs**

Modulator, Non-Coherent FSK Detector, BPSK- Modulator, Coherent BPSK Detection. Principles of QPSK, Differential PSK and QAM. **Laboratory Sessions/ Experimental Learning:** 1. Analyze constellation of 16-QAM Using MATLAB **Applications:** CDMA, WiMAX (16d, 16e), telemetry, caller ID, garage door openers, wireless communication, mobile communication and satellite communication, LANs, Bluetooth, RFID, GPS, Wi-Fi, etc.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Explain the concepts of analog modulation techniques such as amplitude, modulations and its variations like DSB-SC and SSB-SC.
CO2	Analyze frequency modulation and compute performance of different types of noise.
CO3	Apply the concepts of noise in analog modulation and analysis of pre-emphasis and de-emphasis circuit.
CO4	Analyze the signal space representation of digital signals.
CO5	Analyze the performance of a baseband and pass band digital communication system and spread spectrum techniques.
Text Books:	
1.	Simon Haykins & Moher, Communication Systems, 5th Edition, John Wiley, India Pvt. Ltd, 2010, ISBN 978 – 81 – 265 – 2151 – 7.
2.	Simon Haykins, "An Introduction to Analog and Digital Communication", John Wiley
Reference Books:	
1.	B P Lathi and Zhi Ding, Modern Digital and Analog Communication Systems, Oxford University Press., 4th edition, 2010, ISBN: 97801980738002.

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Theory for 50 Marks

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Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: III		
ARTIFICIAL INTELLIGENCE AND MACHINE LEARNING		
Course Code:	**MVJ22VL362**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Understand the AI foundations and applications.	
2	Apply machine learning algorithms to analyze and interpret real-world datasets.	
3	Solve problems by searching.	
4	Analyze advanced problem solving paradigms and knowledge representation.	
5	Implement various learning algorithms, such as backpropagation and gradient descent, to optimize neural network parameters.	

UNIT 1	
Introduction: What is artificial intelligence? What Is AI? The Foundations of Artificial Intelligence, The History of Artificial Intelligence, The State of the Art. **Heuristic Search Techniques:** Generate and test, Hill Climbing, Best First Search, Problem Reduction, Constraint Satisfaction, Means-ends Analysis. **Laboratory Sessions/ Experimental Learning:** 1. Find the shortest path from a start node to a goal node in a maze using heuristic search technique. **Applications:** Used in AI for games such as chess, checkers, and Go to determine optimal moves.	**8Hrs.**
UNIT 2	
Knowledge Representation: Knowledge representation issues, predicate logic, representation knowledge using rules. **Concept Learning:** Concept learning task, concept learning as search, find-S algorithm, candidate elimination algorithm, inductive bias of candidate elimination algorithm**.** **Laboratory Sessions/ Experimental Learning:**	**8Hrs.**

1. Apply the concept learning paradigm in machine learning, specifically using the Find-S algorithm to identify the most specific hypothesis from a given dataset. **Applications:** Expert systems use knowledge representation to model medical expertise for diagnosing diseases based on symptoms, medical history, and tests.	
UNIT 3	
Decision Tree Learning: Introduction, decision tree representation, appropriate problems, ID3 algorithm. **Artificial Neural Network:** Introduction, NN representation, appropriate problems, perceptrons, backpropagation algorithm. **Laboratory Sessions/ Experimental Learning:** 1. Apply decision tree representation in machine learning by building and visualizing a decision tree classifier. **Applications:** Decision trees help in diagnosing diseases based on patient symptoms, medical history, and test results.	**8Hrs.**
UNIT 4	
Bayesian Learning: Introduction, Bayes theorem, Bayes theorem and concept learning, ML and LS error hypothesis, ML for predicting, MDL principle, Bates optimal classifier, Gibbs algorithm, Navie Bayes classifier, BBN, EM Algorithm **Laboratory Sessions/ Experimental Learning:** 1. Apply the concept of least squares error hypothesis in machine learning, specifically using linear regression to predict outcomes based on input features. **Applications:** Used to model the probability of fraudulent activities based on historical transaction data and patterns.	**8Hrs.**
UNIT 5	
Instance-Base Learning: Introduction, k-nearest neighbour learning, locally weighted regression, radial basis function, case-based reasoning, reinforcement learning: Introduction, learning task, Q-learning. **Laboratory Sessions/ Experimental Learning:**	**8Hrs.**

1. Apply the K-nearest neighbors (KNN) algorithm in machine learning, using it to classify a dataset and evaluate its performance. **Applications:** k-NN**:** Movie Recommendations, Medical Diagnosis, Image Recognition. Locally Weighted Regression**:** Sales Forecasting, Stock Market Prediction, Financial Forecasting.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Understand the fundamental principles of artificial intelligence and machine learning.
CO2	Apply machine learning algorithms such as linear regression, decision trees, to develop and train models using real-world datasets.
CO3	Implement techniques for data preprocessing to prepare datasets for machine learning tasks.
CO4	Apply the knowledge of searching and reasoning techniques for different applications.
CO5	Analyze the performance of neural network models by evaluating metrics such as accuracy, loss, precision.

Text Books:	
1.	Tom M Mitchell, "Machine Learning", 1st Edition, McGraw Hill Education, 2017.
2.	Elaine Rich, Kevin K and S B Nair, "Artificial Intelligence", 3rd Edition, McGraw Hill Education, 2017.
Reference Books:	
1.	Saroj Kaushik, Artificial Intelligence, Cengage learning.
2.	Stuart Rusell, Peter Norving, Artificial Intelligence: A Modern Approach, Pearson Education 2nd Edition.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50

marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
CO1	**3**	**3**	**3**	**2**	**-**	**1**	**-**	**-**	**1**	**-**	**-**	**1**	**2**	**1**
CO2	**3**	**3**	**3**	**2**	**-**	**1**	**-**	**-**	**1**	**-**	**-**	**1**	**2**	**1**
CO3	**3**	**3**	**3**	**2**	**-**	**1**	**-**	**-**	**1**	**-**	**-**	**1**	**2**	**1**
CO4	**3**	**3**	**3**	**2**	**-**	**1**	**-**	**-**	**1**	**-**	**-**	**1**	**2**	**1**
CO5	**3**	**3**	**3**	**2**	**-**	**1**	**-**	**-**	**1**	**-**	**-**	**1**	**2**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: III		
COMPUTER ORGANIZATION & ARCHITECTURE		
Course Code:	**MVJ22VL363**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**

Course Learning Objectives: The students will be able to	
1	Explain the basic sub-systems of a computer, their organization, structure and operation.
2	Apply knowledge of instruction set architectures to design and implement basic assembly language programs for different processor architectures.
3	Analyze the performance of computer systems by examining factors such as pipelining, caching strategies, and parallelism.
4	Describe memory hierarchy and concept of virtual memory.
5	Analyze the design and operation of memory systems by evaluating cache coherence protocols, memory mapping techniques, and virtual memory management strategies.

UNIT 1	
Basic Structure of Computers: Computer types, functional units, basic operational concepts, bus structures, software, performance – processor clock, basic performance equation. **Machine Instructions and Programs:** Numbers, arithmetic operations and characters, IEEE standard for floating point numbers, memory location and addresses, memory operations, instructions and instruction sequencing. **Laboratory Sessions/ Experimental Learning:** 1. Understanding various parts of CPU of a PC. 2. Study of microprocessor and understanding of its various instruction **Applications:** Understand the functionality of the various units of computer.	**8Hrs.**
UNIT 2	
Prerequisite: *Number systems* **Addressing Modes:** Assembly language, basic input and output operations, stacks and queues, subroutines, additional instructions.	**8Hrs.**

Laboratory Sessions/ Experimental Learning: 1. Write an ALP to find the sum of two numbers and verify if the sum is an even or odd number and simulate the output. 2. Write an ALP to transfer a block of data from one location to other and simulate the output. **Applications:** Project based on microprocessor.	
UNIT 3	
Input/Output Organization: Accessing I/O devices, interrupts – interrupt hardware, enabling and disabling interrupts, handling multiple devices, controlling device requests, direct memory access, and buses. **Laboratory Sessions/ Experimental Learning:** Study any one input/output device and examine its various input output ports details. **Applications:** Interfacing of peripheral devices	**8Hrs.**
UNIT 4	
Memory System: Basic concepts, semiconductor RAM memories- Internal organization of memory chips, static memories, asynchronous DRAMS, read only memories, cache memories, mapping functions, replacement algorithm, virtual memories, secondary storage-magnetic hard disks. **Laboratory Sessions/ Experimental Learning:** Implement and simulate a simple memory unit which is capable of reading and writing data within a single clock cycle. **Applications:** Understanding the various memories.	**8Hrs.**
UNIT 5	
Basic Processing Unit: Some fundamental concepts, execution of a complete instruction, multiple bus organization, hardwired control, micro programmed control, pipelining, basic concepts, role of cache memory, pipeline performance. **Laboratory Sessions/ Experimental Learning:** Evaluate the possible control sequence for implementing a multiplication instruction using registers for a single bus organization **Applications:** Microprocessor	**8Hrs.**
Course Outcomes: After completing the course, the students will be able to	

CO1	Identify the functional units of the processor and the factors affecting the performance of a computer.
CO2	Demonstrate the ability to classify the addressing modes, instructions sets and design programs.
CO3	Understand the different ways of accessing an input / output device including interrupts.
CO4	Analyze the organization of different types of semiconductor and other secondary storage memories.
CO5	Analyze the simple processor organization based on hardwired control and micro programmed control.

Text Books:	
1.	Carl Hamacher, ZvonkoVranesic, SafwatZaky: "Computer Organization", 6th Edition, Tata McGraw Hill, 2011.
Reference Books:	
1.	Andrew S. Tanenbaum, Todd Austin, "Structured Computer Organization", 6th Edition, Pearson, 2013.
2.	David A. Patterson, John L. Hennessy: "Computer Organization and Design – The Hardware / Software Interface ARM Edition", 4th Edition, Elsevier.
3.	William Stallings: "Computer Organization & Architecture", 7th Edition, PHI.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the

entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
CO1	**3**	**3**	**3**	**2**	**-**	**1**	**-**	**-**	**1**	**-**	**-**	**1**	**2**	**1**
CO2	**3**	**3**	**3**	**2**	**-**	**1**	**-**	**-**	**1**	**-**	**-**	**1**	**2**	**1**
CO3	**3**	**3**	**3**	**2**	**-**	**1**	**-**	**-**	**1**	**-**	**-**	**1**	**2**	**1**
CO4	**3**	**3**	**3**	**2**	**-**	**1**	**-**	**-**	**1**	**-**	**-**	**1**	**2**	**1**
CO5	**3**	**3**	**3**	**2**	**-**	**1**	**-**	**-**	**1**	**-**	**-**	**1**	**2**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: III		
SENSOR TECHNOLOGY		
Course Code:	**MVJ22VL364**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**

Course Learning Objectives: The students will be able to	
1	Understand various technologies associated in manufacturing of sensors.
2	Provide better familiarity with different sensors and their applications in real life.
3	Acquire knowledge about types of sensors used in modern digital systems.
4	Evaluate the technological and physical limitations of a specific sensor.
5	Propose a suitable sensor for a given measurement situation.

UNIT 1	
Prerequisite: *Basic Electronics, Knowledge on physical quantities.* **Sensors Fundamentals and Characteristics:** General concepts and terminology, sensor classification, static characteristics, dynamic characteristics, materials for sensors, microsensor technology. **Laboratory Sessions/ Experimental Learning:** 1. To understand the fundamental concepts and characteristics of temperature and pressure sensors including their static and dynamic characteristics **Applications:** Weather stations, air quality monitoring, climate research	**8Hrs.**
UNIT 2	
Temperature Sensors: Basic Concepts, temperature scale, standard temperature points, thermistor sensors, thermocouple sensors, pyrometer, radiation thermometer, Temperature sensor applications **Position Measurement Sensors:** Principle of position measurement, inductive sensors, capacitive sensors, capacitive and inductive sensor applications, hall effect sensors **Laboratory Sessions/ Experimental Learning:** 1. Measure resistance at various temperatures in thermistors	**8Hrs.**

Applications: Industrial Process Control**:** Furnace temperature monitoring. Environmental Monitoring: Weather stations. Medical Diagnostics**:** Body temperature measurement. Automotive Applications: Engine temperature monitoring.	
UNIT 3	
Strain Gauge Sensors: Transfiguration and measurement methods, resistive metal probe, piezoresistive silicon sensors **Pressure Measurement Sensors:** Pressure measurement principles, characteristics of pressure sensors, types of pressure sensors, piezoelectric sensors, magnetoresistive sensors, pressure measurement sensor applications **Laboratory Sessions/ Experimental Learning:** 1. Compare measured pressures with reference gauge data. **Applications:** Bridge and Building Monitoring	**8Hrs.**
UNIT 4	
Optical Sensors: Luminescent sensors, photoresistors, photoelectric cells, classification of optical sensors **Fluid-flow Measurement sensors:** Flow measurement methods, types of sensors used to measure fluid flows, level sensors, flow measurement by pressure difference **Laboratory Sessions/ Experimental Learning:** **1.** Study static and dynamic characteristics of each optical sensor. **Applications:** Flow meters are used to monitor and control water flow in treatment processes.	**8Hrs.**
UNIT 5	
Motion Sensors: Resistive potentiometer, LVDT, Eddy current sensor, Piezoelectric accelerator sensor **Proximity sensors:** Introduction, inductive proximity sensors, capacitive proximity sensors, optical proximity sensors, ultrasonic proximity sensors **Laboratory Sessions/ Experimental Learning:** 1. Evaluate the performance of inductive, capacitive, optical, and ultrasonic proximity sensors.	**8Hrs.**

Applications: LVDTs used for precise position control in robotic arms for manufacturing tasks.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Understand the concept of sensors and its characteristics.
CO2	Explain the working principles of primary and resistive sensors.
CO3	Understand the inductive, capacitive and Electromagnetic sensors and its applications.
CO4	Identify alternative methods to measure common quantities such as temperature, pressure, force and acceleration.
CO5	Select appropriate sensors used for various applications.

Text Books:	
1.	Ramon Pallas & John G.Webster, "Sensors and signal conditioning", John Wiley & Sons., 2nd Edition.
2.	J. Fraden, "Handbook of Modern Sensors: Physical, Designs, and Applications", AIP Press, Springer, 3rd Edition
Reference Books:	
1.	D. Patranabis, "Sensors and Transducers", PHI Publication, 2nd Edition, New Delhi.
2.	Webster John G, "Instrumentation and sensors Handbook", CRC Press, 1st Edition.
3.	Shawhney A.K., "Electrical and Electronics Measurements and Instrumentation", Dhanpat Rai & Sons.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
CO1	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: IV		
FPGA BASED SYSTEM DESIGN USING VERILOG HDL		
Course Code:	**MVJ22VL41**	**CIE Marks:100**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 100**
Hours:	**40L**	**SEE Duration: 3 Hrs**

Course Learning Objectives: The students will be able to	
1	Explain the fundamental concepts of FPGA architecture, describing the components such as logic cells, interconnect resources, and configurable I/O blocks that constitute an FPGA.
2	Apply Verilog HDL to implement digital circuits on FPGA platforms.
3	Analyze the impact of design choices on FPGA resource usage and power consumption by examining synthesis reports, power analysis tools, and performance profiling.
4	Develop proficiency in writing synthesizable Verilog code for combinational and sequential logic.
5	Model designs using IP-based methodologies and tools.

UNIT 1	
Introduction to Programmable Logic Devices: Introduction to programmable logic and comparison with full custom, semi-custom, and gate array design flow. **CPLD:** Working principle, architecture, I/O block, macrocells, programming, features, examples. **FPGA:** Working principle, architecture, I/O block, CLB, embedded memory, clock management, DSP capability, programming, features, examples, FPGA design flow, prototyping solution, need for hardware description languages and implementation and verifications of digital logics on FPGA platform to prove FPGA design flow. Distinguish between HDL based digital logic design and test-bench for verifications. **Laboratory Sessions/ Experimental Learning:** 1. Understand the basics of PLDs, including their architecture and use in digital logic design. **Applications:** To design accelerator for specific application like ALU, Floating point	**8Hrs.**

processing Unit (FPU)	
UNIT 2	
Verilog HDL Language: Importance and popularity of verilog HDL, typical design flow. Hierarchical modeling concepts: Top to bottom and bottom to top. Difference between design and test-bench writing using verilog, **Lexical Conventions:** Whitespace, comments, operators, number specifications, string, identifiers, keywords. **Data Types:** Value set, nets, registers, vectors, integer, real, and time register data, arrays, memories, parameters and string. System tasks and compiler directives, module, ports, and hierarchical names. **Laboratory Sessions/ Experimental Learning:** 1. Create simple verilog modules to demonstrate the use of verilog data types. **Applications:** Digital logics Adder, Subtractor etc.	**8Hrs.**
UNIT 3	
Design Modeling Techniques: Gate/Structural level modeling: Highlights of structural description, organization of structural description, half adder and full adder design using structural description, half subtractor and full subtractor design using structural description. **Data Flow Level Modeling:** Highlights of data-flow description, signal declaration and assignment statement, constant declaration and constant assignment statements, assigning a delay time to the signal-assignment statement. **Behavioral Level Modeling:** Behavioral description highlights, structure of the verilog behavioral description, sequential statements: If statement, the case statement, verilog casex and casez, the wait-for statement, the loop statement: for-loop, while-loop, repeat, forever. **Switching Level Modeling:** Highlights of switching level description, MOS, CMOS switches, NOR and NAND gate implementation using switching flow. Tasks and Functions, timing and delays, modular test benches **Laboratory Sessions/ Experimental Learning:** 1. Design a 4-bit arithmetic logic unit (ALU) using behavioral modeling. **Applications:** Algorithms: FSMs, ECC	**8Hrs.**
UNIT 4	

Synthesis Basics: Highlights of synthesis, synthesis information from module, mapping always in the hardware domain, mapping the signal-assignment statement to gate level, mapping logical operators, mapping the IF statement, mapping the case statement, mapping the loop statement. **Implementation:** Mapping, placement and routing. **Laboratory Sessions/ Experimental Learning:** 1. Analyze the synthesis report to understand the resource utilization and timing summary**.** **Applications:** FPGA based prototyping	**8Hrs.**
UNIT 5	
IP-Based Digital Logic Design and Logic Validation: Basics of AXI interfacing, IP-based counter implementation, IP-based different clock generator, FIFO, and BRAM. **Real Time Logic Validations:** Integrated logic analyzer (Xilinx ILA IP) and virtual input and output (VIO). **Laboratory Sessions/ Experimental Learning:** 1. Analyze timing diagrams and understand the signaling involved in AXI transactions. **Applications:** Embed ILA IP to monitor internal signals and debug the system in real-time.	**8Hrs.**

Course Outcomes: After completing the course, the students will be able to	
CO1	Explain the basic architecture and functioning of FPGAs.
CO2	Develop synthesizable Verilog HDL code for combinational and sequential logic circuits.
CO3	Make use of simulation tools to debug and validate Verilog HDL code.
CO4	Understand the FPGA design flow, including synthesis, placement, and routing.
CO5	Develop AXI-based interfaces for high-speed communication within FPGA designs.

Text Books	
1.	Palnitkar, S. "Verilog HDL: A guide to Digital Design and Synthesis" 2nd ed. Pearson.
2.	Sass, Ronald, and Andrew G. Schmidt, "Embedded systems design with platform FPGAs: Principles and practices", Morgan Kaufmann.

Reference Books	
1.	J. A Bhasker, “System Verilog Primer” 1st Indian ed. B.S. Publication.
2.	Steve Kilts, Advanced FPGA design: architecture, implementation, and optimization” John Wiley & Sons.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom’s taxonomy level.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**
CO2	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**
CO3	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**
CO4	**3**	**2**	**2**	**-**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**
CO5	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: IV		
NETWORK THEORY		
Course Code:	**MVJ22VL42**	**CIE Marks: 50**
Credits:	**L: T:P: 3:0:2**	**SEE Marks: 50**
Hours:	**40L+26P**	**SEE Duration: 3 Hrs.**

Course Learning Objectives: The students will be able to

1	Understand the basic network concepts emphasizing source transformation, mesh and nodal techniques to solve for resistance/impedance, voltage, current and power.
2	Apply Thevenin's, Millman's, superposition, reciprocity, maximum power transfer and Norton's Theorems in solving the problems related to electrical circuits.
3	Analyze the frequency response of series and parallel combination of passive components as resonating circuits.
4	Describe the behavior of RLC circuits in the time and frequency domain.
5	Analyze the two port network parameters like Z, Y, T and h and their inter-relationships.

UNIT-I	
Basic Concepts: Introduction, practical sources, source transformations, star – delta transformation, loop and node analysis with linearly dependent and independent sources for DC networks, concepts of super node and super mesh. **Laboratory Sessions/ Experimental Learning:** 1. Find the current through and voltage across the load in the circuit. **Applications:** Simplification and analysis of analog circuits, microwave circuit analysis.	**8 Hrs**
UNIT-II	
Graph Theory and Network Equations: Graph of a network, trees, co-trees and loops, incidence matrix, cut-set matrix, tie-set matrix and loop currents, number of possible trees of a graph, analysis of networks, duality. **Laboratory Sessions/ Experimental Learning:** 1. Understand and apply graph theory concepts such as trees, co-trees, loops, incidence matrices, cut-set matrices, tie-set matrices, and loop currents to the analysis of electrical networks.	**8 Hrs**

Applications: Simplification and analysis of analog circuits, microwave circuit analysis.	
UNIT-III	
Network Theorems: Superposition theorem, Millman's theorem, Thevenin's and Norton's theorems, reciprocity theorem, maximum power transfer theorem. **Laboratory Sessions/ Experimental Learning**: 1. Verify superposition theorem for a circuit. **Applications:** Simplification and analysis of analog circuits, microwave circuit analysis.	**8 Hrs**
UNIT-IV	
Transient Behaviour and Initial Conditions: Behaviour of circuit elements under switching condition and their representation, evaluation of initial and final conditions in RL, RC and RLC circuits for DC excitations, applications of Laplace transforms in circuit analysis. **Laboratory Sessions/ Experimental Learning:** 1. Plot the response of a series RLC circuit. **Applications:** In the analysis of transmission lines and waveguides.	**8 Hrs**
UNIT-V	
Two Port Network Parameters: Introduction, open circuit impedance parameter, short circuit admittance parameter, hybrid parameters, transmission parameter, relationship between parameters. **Laboratory Sessions/ Experimental Learning:** 1. Plot the frequency response characteristics for a series RL, RC circuit. 2. Plot the frequency response characteristics for a parallel RL circuit. 3. Measure two port parameters for a given network **Applications:** For analysis of communication systems and antennas.	**8 Hrs**

Course Outcomes: After completing the course, the students will be able to	
CO1	Apply network simplification techniques to calculate currents and voltages in a circuit.
CO2	Describe the network problems using graphical methods.

CO3	Apply network theorems to simplify the complex circuits.
CO4	Examine and differentiate between transient and steady-state responses of electrical circuits to various inputs, using techniques such as differential equations and Laplace transforms.
CO5	Analyze the given network using specified two port network parameters like Z or Y or T or h and evaluate the frequency response related parameters through the RLC elements, in resonant circuits.

LIST OF EXPERIMENTS

S. No.	**Experiment Name**
1.	Apply the kirchoff's law for finding current in a complex electrical circuit.
2.	Verification of Norton and maximum power transfer theorems in ac circuits.
3.	Apply the Thevenin theorem for finding current in a complex electrical circuit.
4.	Determination of transient response of current in RL and RC circuits with step voltage input.
5.	Determination of transient response of current in RLC circuit with step voltage input for under damp, critically damp and over damp cases.
6.	Determination of the equivalent parameters of series connection of two port network.
7.	Determination of impedance and admittance for series and parallel RLC circuits.
8.	Analyze circuit in s-domain (Laplace Transform)

Text Books	
1.	M.E. Van Valkenberg, "Network analysis", Prentice Hall of India, 3rd edition, ISBN: 9780136110958.
2.	Roy Choudhury, "Networks and systems", 2nd edition, New Age International Publications, ISBN: 9788122427677.
Reference Books	
1.	Hayt, Kemmerly and Durbin ―Engineering Circuit Analysis", TMH 7th Edition, 2010.
2.	J. David Irwin /R. Mark Nelms, "Basic Engineering Circuit Analysis", John Wiley, 8th edition.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

Laboratory- 50 Marks

Experiment Conduction with proper results is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

Semester: IV		
ELECTROMAGNETIC FIELD THEORY		
Course Code:	**MVJ22VL43**	**CIE Marks:50**
Credits:	**L:T:P:S 3:0:0:Y**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Understand the physical significance of Biot-Savart's Law, Amperes' circuital law and Stokes' theorem for different current distributions.	
2	Apply mathematical methods, including vector calculus and differential equations, to solve problems related to electromagnetic fields.	
3	Analyze electromagnetic wave propagation by evaluating wave equations, polarization states, and propagation characteristics in different media.	
4	Understand the concepts of Smith Chart for impedance matching.	
5	Analyze the interaction between electromagnetic fields and materials by examining concepts such as dielectric and magnetic properties.	

UNIT 1	
Prerequisites: *Vector algebra, coordinate systems (Rectangular coordinate system, cylindrical coordinate system and spherical coordinate system), gradient, divergence and curl.* **Electrostatics: Coulomb's Law, Electric Field Intensity, Flux Density and Potential:** Coulomb's law, electric field intensity, field due to line charge, field due to Sheet of charge, field due to continuous volume charge distribution, electric flux, electric flux density, electric potential, potential difference, relation between electric field intensity (E) & potential (V), potential gradient, electric dipole, energy density in electrostatic fields. **Laboratory Sessions/ Experimental Learning:** 1. Determine the electric field intensity at a point due to uniform linear charge (ρ L) and point charges using MATLAB. 2. Determine the electric field intensity at a point due to surface charge using MATLAB.	**8 Hrs.**

3. Determine the potential difference between two points on a ring having linear charge density, ρ L using MATLAB. **Applications:** The Van de Graaff generator, Xerography, Ink Jet Printers and Electrostatic Painting, Smoke Precipitators and Electrostatic Air Cleaning.	
UNIT 2	
Gauss' law, Divergence, Poisson's and Laplace's Equations: Gauss law, Maxwell's first equation, application of Gauss' law, divergence theorem, current, current density, conductor, the continuity equation, boundary conditions (dielectric-dielectric, conductor-dielectric, conductor-free space), Poisson's and Laplace's equations. **Laboratory Sessions/ Experimental Learning:** 1. Evaluate the current flowing through a given surface using MATLAB. 2. Verify the divergence theorem using MATLAB. **Applications:** Used for calculation electrical field for a symmetrical distribution of charges.	**8 Hrs.**
UNIT 3	
Magnetostatics: Steady magnetic field-Biot-Savart law, Ampere's circuital law, Curl, Stokes' theorem, Gauss's law for magnetic fields, magnetic flux and magnetic flux density, Maxwell's equations for static fields, magnetic scalar and vector Potentials. **Magnetic Forces and Magnetic Materials:** Force on a moving charge and differential current element, force between differential current elements, magnetization, magnetic susceptibility, permeability, magnetic boundary conditions, inductances, magnetic energy, magnetic circuit. **Laboratory Sessions/ Experimental Learning:** 1. Determine the magnetic field intensity at a point due to magnetic field using MATLAB. **Applications:** Motors, Generators, Loudspeakers, MRI.	**8 Hrs.**
UNIT 4	
Time Varying Fields and Electromagnetic Wave Propagation: Time varying fields & Maxwell's equations, Faraday's law, transformer and motional electro - motive forces, displacement current, Maxwell's equation in differential and integral form, time varying potentials.	**8 Hrs.**

Electromagnetic Wave Propagation: Derivation of wave equations from Maxwell's equations, relation between E and H, Wave propagation in - lossy dielectrics, lossless dielectrics, free space and good conductor, skin-effect, Poynting theorem. **Laboratory Sessions/ Experimental Learning:** 1. Determine the parameters of wave using MATLAB. **Applications:** Optoelectronics.	
UNIT 5	
Transmission Line: Introduction, transmission line parameters, transmission line equations, input impedance, standing wave ratio and power, Smith Chart basic fundamentals, types of transmission lines - coaxial line, strip line, micro strip line. **Applications of Transmission Line**: Impedance matching and tuning: Single stub tuning, double stub tuning, and the quarter wave transformer. **Laboratory Sessions/ Experimental Learning:** 1. Simulation of micro strip transmission line using FEKO software. **Applications:** Telephone, Cable TV, Broadband network	**8 Hrs.**

Course Outcomes: After completing the course, the students will be able to	
CO1	Solve problems on electrostatic force, electric field due to point, linear, surface charge and volume charges.
CO2	Apply Gauss law to evaluate electric fields due to different charge distributions by using Divergence Theorem.
CO3	Apply Biot-Savart's and Ampere's laws for evaluating magnetic field for different current configurations.
CO4	Apply Maxwell's equations for time varying fields and evaluate power associated with EM waves using Poynting theorem.
CO5	Design electromagnetic devices and systems, such as antennas and transmission lines, while optimizing performance characteristics such as impedance matching and radiation patterns.

Text Books:	
1.	Matthew N. O. Sadiku, "Elements of Electromagnetics", Oxford University Press, Edition VII, 2018.

2.	David M Pozar, “Microwave Engineering”, John Wiley & Sons, Inc., 4th edition, 2014.
Reference Books:	
1.	W.H. Hayt. J.A. Buck & M Jaleel Akhtar, “Engineering Electromagnetics”, Tata McGraw – Hill, Edition VIII, 2014.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom’s taxonomy level.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: IV		
VERILOG HDL LABORATORY		
Course Code:	**MVJ22VLL44**	**CIE Marks: 50**
Credits:	**L:T:P:0:0:2**	**SEE Marks: 50**
Hours:	**26P**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Understand architectures of FPGA , CPLD and different IC design flow.	
2	Apply verilog HDL design flow and hierarchical modeling to design various digital circuits.	
3	Design and verify circuits using various verilog modeling techniques.	
4	Grasp the synthesis process from high-level design to hardware implementation.	
5	Implement and validate designs using IP-based methodologies and tools.	

LABORATORY SESSIONS	
PART A	
Exp. No	**Experiment Name**
1.	Write Verilog program for the following combinational logic, verify the design using test bench and perform the synthesis by downloading the design on to FPGA device. a. Structural modeling of Full adder using two half adders and or Gate b. BCD to Excess-3 code converter
2.	Write Verilog program for the following Sequential Circuits, verify the design using test bench and perform the synthesis by downloading the design on to FPGA device. a. Mod-N counter b. Random sequence counter
3.	Write Verilog program for the following Sequential Circuits, verify the design using test bench and perform the synthesis by downloading the design on to FPGA device. a. SISO and PISO shift register b. 4-Bit Linear Feedback shift register b. Barrel Shifter

4.	Write Verilog program for the following Digital Circuits, verify the functionality using test bench and perform the synthesis by downloading the design on to FPGA device. a. Ring Counter b. Johnson Counter
5.	Write Verilog program for the following Digital Circuits, verify the functionality using test bench and perform the synthesis by downloading the design on to FPGA device. a. 4-Bit Ripple Carry Adder b. 4-bit Array Multiplication. c. 4-bit Booth Multiplication
PART B	
6	Write a Verilog code to design a clock divider circuit that generates 1/2, 1/3rdand 1/4thclock from a given input clock. Port the design to FPGA and validate the Functionality through ILA.
7	Generate 3 different clock frequencies using predefined IP and validate using oscilloscopes.
8	Write a Verilog code to interface LED and display HDL on the LED display and also validate all output using VIO IP before implementations
9	Design a FSM to detect 1010 patterns and validate real time detection of patterns using ILA IP
10	Write Verilog code to convert an analog input of a sensor to digital form by interfacing ADC to display the same on a suitable display like set of simple LEDs like 7-Segment display digits.
11	Interface a DAC to FPGA and write Verilog code to generate Square wave of Frequency F KHz. Modify the code to down sample the frequency to F/2 KHz. Display the original and Down sampled signals by connecting them to an Oscilloscope.
Course Outcomes: After completing the course, the students will be able to	
CO1	Develop proficiency in writing Verilog code for modelling digital systems at various levels of abstraction (behavioral, dataflow, and structural).

CO2	Apply Verilog HDL to design and simulate basic digital circuits such as logic gates, multiplexers, and flip-flops, using simulation tools to verify circuit functionality.
CO3	Analyze the behavior of Verilog-based designs by evaluating simulation results, identifying and debugging errors in the Verilog code, and optimizing designs for performance.
CO4	Design and implement complex digital systems, such as finite state machines (FSMs)
CO5	Implement Verilog designs on Field-Programmable Gate Arrays (FPGAs) and understand the FPGA design flow.

CO-PO-PSO Mapping														
CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
CO1	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**
CO2	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**
CO3	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**
CO4	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**
CO5	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**

High-3, Medium-2, Low-1

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B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: IV		
CONTROL SYSTEMS		
Course Code:	**MVJ22VL451**	**CIE Marks:100**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 100**
Hours:	**40L**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Explain the fundamental principles and components of control systems.	
2	Apply control theory to model dynamic systems using differential equations and state-space representations.	
3	Analyse the response of first and second order systems using standard test signals and analyse steady state error.	
4	Analyse stability of systems using RH criteria, root locus, Nyquist, Bode plot and polar plot.	
5	Design controllers such as PID, lead-lag, and state feedback controllers to achieve desired system performance specifications.	

UNIT 1	
Introduction to Control Systems: Open loop and closed loop systems, types of feedback, differential equation of physical systems – Mechanical systems, electrical systems, analogous systems. **Block Diagrams and Signal Flow Graphs:** Transfer functions, block diagram algebra and signal flow graphs. **Laboratory Sessions/ Experimental Learning:** 1. Determine and plot poles and zeros from the transfer function using MATLAB. **Applications:** Electric hand drier, automatic washing machine, DC motor, automatic electric iron, voltage stabilizer**.**	**8Hrs.**
UNIT 2	
Time Response of Feedback Control Systems: Standard test signals, unit step response of first and second order systems. Time response specifications of first order systems, time response specifications of second order systems for underdamped system, steady state errors and error constants.	**8Hrs.**

Introduction to Controllers: P, PI, PD and PID Controllers. **Laboratory Sessions/ Experimental Learning:** 1. Obtain step and impulse response of a unity feedback first order system for a given forward path transfer function using MATLAB. 2. Obtain step and impulse response of a unity feedback second order system for a given forward path transfer function using MATLAB. **Applications:** Industrial control systems	
UNIT 3	
Stability Analysis Using RH Criteria and Root Locus: Concepts of stability, necessary conditions for stability, Routh Hurwitz stability criterion, relative stability analysis, introduction to root-locus techniques, the root locus concepts, construction of root loci. **Laboratory Sessions/ Experimental Learning:** 1. Obtain root locus plot of the system for a given forward path transfer function using MATLAB. **Applications:** Used to determine the dynamic response of a system.	**8Hrs.**
UNIT 4	
Stability Analysis using Nyquist Criteria and Bode Plots: Polar plot, Nyquist stability criterion, Nyquist plots, Bode plots, gain and phase margin. **Laboratory Sessions/ Experimental Learning:** 1. Obtain Bode plot of the system for a given forward path transfer function using MATLAB. 2. Obtain Nyquist plot of the system for a given forward path transfer function using MATLAB. **Applications:** To determine a stability of a system.	**8Hrs.**
UNIT 5	
Introduction to State Variable Analysis: Concepts of state, state variable and state models for electrical systems, solution of state equations, state transition matrix and its properties. lag, lead and lag lead compensation. **Laboratory Sessions/ Experimental Learning:**	**8Hrs.**

1. Determining the solution of state equations using MATLAB. **Applications:** State variables are used to describe the future response of a d+ynamic response.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Apply mathematical models to represent and simulate the behavior of dynamic systems.
CO2	Analyze transient and steady state response of second order systems using standard test signals and analyze steady state error.
CO3	Analyze the stability of the systems by applying RH criteria and root locus techniques.
CO4	Analyze the stability of the system using frequency domain techniques such as Nyquist and Bode plots.
CO5	Design and implement controllers, such as proportional-integral-derivative (PID) controllers, lead-lag compensators, and state feedback controllers.

Text Books:	
1.	Nagarath and M.Gopal, Control Systems Engineering, New Age International (P) Limited, Publishers, Fifth edition, ISBN: 81-224-2008.
2.	Modern Control Engineering, K.Ogata, Pearson Education Asia/PHI, 4th Edition, ISBN 978-81-203-4010-7.
Reference Books:	
1.	Automatic Control Systems‖, Benjamin C. Kuo, John Wiley India Pvt. Ltd., 8th Edition.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: IV		
INDUSTRIAL ELECTRONICS		
Course Code:	**MVJ22VL452**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40 L**	**SEE Duration: 03 Hours**

Course Learning Objectives: The students will be able to

1	Explain broad types of industrial power devices, there structure, and its characteristics.
2	Design and analyse the broad categories of power electronic circuits.
3	Explain various types of MEMs devices, principle of operation and construction.
4	Familiarize with soft core processors and computer architecture
5	Apply protective methods for devices and circuits.

UNIT-I

Industrial Power Devices: General purpose power diodes, fast recovery power diodes, schottky power diodes, silicon carbide power diodes, Power MOSFETs, Steady state characteristics, switching characteristics, silicon carbide MOSFETs, COOLMOS, Junction field effect transistors, operation and characteristics of JFETs, Silicon Carbide JFET structures, Bipolar Junction Transistors, Steady state characteristics, switching characteristics, silicon carbide BJTs, IGBT, silicon carbide IGBTs **Laboratory Sessions/ Experimental Learning:** **1.** To understand the steady-state and switching characteristics of various industrial power devices, including power diodes, MOSFETs, JFETs, BJTs, and IGBTs, and explore their applications in industrial settings. **Applications:** High-efficiency power conversion system can be deployed in various industrial applications	**8 Hrs**

UNIT-II

Power Electronics Circuits: Thyristor, Thyristor characteristics, two transistor model. Controlled Rectifiers – Single phase full converter with R and RL load, Single phase dual converters, and Three phase full converter with RL load. Switching mode regulators – Buck Regulator, Boost regulator, Buck – Boost regulator, comparison of regulators	**8 Hrs**

Laboratory Sessions/ Experimental Learning: **1.** Use the semiconductor parameter analyzer to measure the thyristor's I-V characteristics. **Applications:** The solar power inverter system can be deployed in residential and commercial settings to harness solar energy efficiently and reduce dependency on conventional power sources.	
UNIT-III	
Inverters – Principle of operation, Single phase bridge inverter, Three phase inverter with 180 and 120 degree conduction, Current source inverter. AC voltage controllers – Single phase full wave controller with resistive load, single phase full wave controller with inductive load **Laboratory Sessions/ Experimental Learning:** 1. To understand the principles of operation of inverters and AC voltage controllers, and to analyze the performance of single-phase and three-phase inverters, as well as single-phase full-wave AC voltage controllers with resistive and inductive loads. **Applications:** The UPS system can be deployed in various critical applications such as data centers, medical facilities, industrial automation	**8 Hrs**
UNIT-IV	
MEMS Devices: Sensing and Measuring Principles, Capacitive Sensing, Resistive Sensing, Piezoelectric Sensing, Thermal Transducers, Optical Sensors, Magnetic Sensors, MEMS Actuation Principles, Electrostatic Actuation, Thermal Actuation, Piezoelectric Actuation, Magnetic Actuation, MEMS Devices Inertial Sensors, Pressure Sensors, Radio Frequency MEMS: Capacitive Switches and Phase Shifters, Microfluidic Components, Optical Devices. **MEMS Applications:** Introduction, Industrial, Automotive, Biomedical **Laboratory Sessions/ Experimental Learning:** **1.** To understand the principle of capacitive sensing and to design and test a capacitive MEMS sensor for measuring displacement. **Applications:** The MEMS pressure sensor system can be deployed in vehicles to continuously monitor tire pressure.	**8 Hrs**
UNIT-V	

Protections of Devices and Circuits: Cooling and Heat sinks, Thermal Modeling of Power Switching Devices, Electrical Equivalent Thermal model, Mathematical Thermal Equivalent Circuit, Coupling of Electrical and Thermal Components, Snubber circuits, Voltage protection by Selenium Diodes and Metal oxide Varistors, Current protection, Fusing, Fault current with AC source, Fault current with DC source, Electromagnetic Interference, sources of EMI, Minimizing EMI Generation, EMI shielding, EMI standards **Laboratory Sessions/ Experimental Learning:** **1.** To understand and implement various protection mechanisms for electronic devices and circuits, including thermal management, voltage and current protection, snubber circuits, and electromagnetic interference (EMI) mitigation techniques. **Applications:** The protection system can be deployed in various industrial applications, such as motor drives, renewable energy systems**,** industrial automation	**8 Hrs**

Course Outcomes: After completing the course, the students will be able to	
CO1	Explain different types of industrial power devices such as MOSFET, BJT, IGBT etc, there structure, and its operating characteristics.
CO2	Design and analyse the power electronic circuits such as switch mode regulators, inverters, controlled rectifiers and ac voltage controllers.
CO3	Explain various types of MEMs devices used for sensing pressure, temperature, current, voltage, humidity, vibration etc..
CO4	Familiarize with soft core processors such as ASIC and FPGA.
CO5	Familiarize with computer hardware, software, architecture, instruction set, memory organization, multiprocessor architecture.
Text Books:	
1.	Power Electronics: Devices, Circuits, and Applications, Muhammad H. Rashid, Pearson, 4th International edition.
2.	Fundamentals of Industrial Electronics , Bogdan M. Wilamowski, J. David Irwin, CRC Press.
Reference Books:	

1.	Thomas E. Kissell, Industrial Electronics: Applications for Programmable Controllers, Instrumentation and Process Control, and Electrical Machines and Motor Controls, 3rd edition, Prentice Hall.
2.	Ned Mohan, T.M. Undeland and W.P. Robbins, "Power Electronics: Converters, Applications and Design", Wiley India Ltd.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: IV		
ROBOTICS AND AUTOMATION		
Course Code:	**MVJ22VL453**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40 L**	**SEE Duration: 03 Hours**

Course Learning Objectives: The students will be able to

1	Explain the fundamental concepts and principles of robotics and automation.
2	Apply mathematical and computational techniques to model robotic mechanisms.
3	Analyze the performance and efficiency of robotic systems by evaluating parameters such as accuracy, repeatability, and speed.
4	Analyze basic robotic dynamics, path planning and control problems.
5	Design and implement control algorithms for robotic systems.

UNIT-I

Basic Concepts in Robotics: Definition, anatomy of robot, basic structure of robot, specifications and classification of robot, safety measures in robotics, industrial applications of robots. Drives for robots: Electric, hydraulic and pneumatic. Sensors: Internal-external, contact-non-contact, position, velocity, force, torque, proximity and range. **Laboratory Sessions/ Experimental Learning:** 1. Interface various sensors with Microcontroller. **Applications:** Machine Tending**,** Picking, Packing and Palletizing, painting, all Industrial applications.	**8 Hrs**

UNIT-II

Robot Drivers, Sensors and Vision: Introduction to techniques, image acquisition and processing, different types of grippers- Mechanical, magnetics, vacuum, adhesive, gripper force analysis and gripper design, overview of actuators, power and torque, acceleration and velocity specifications and characteristics of stepper motors, AC motors, DC motors and servomotors. **Laboratory Sessions/ Experimental Learning:**	**8 Hrs**

1. Interface motors using various motor drivers. **Applications:** Industrial application, agriculture robots, surgical robots	
UNIT-III	
Robot Kinematics nd Dynamics: Direct and inverse kinematics for industrial robots for position and orientation, redundancy, manipulator, direct and inverse velocity. Link inertia tensor and manipulator inertia tensor, Newton–Eller formulation for RP and RP manipulators, trajectory planning. **Laboratory Sessions/ Experimental Learning:** 1. Interface servo motors to form gripper. **Applications:** Pick and Place, Excavators, Robotic ARM.	**8 Hrs**
UNIT-IV	
Robot Kinematics: Dynamics and programming methods, robot language classification, robot language structure, kinematics and path planning: Solution of inverse kinematics problem, multiple solution jacobian work envelop, hill climbing techniques, robot programming languages elements and its functions. Simple programs on sensing distance and direction, Line following algorithms, feedback systems. **Laboratory Sessions/ Experimental Learning:** 1. Design algorithm for Maze solving robot. **Applications:** Defence, Surveillance, Autonomous Vehicles	**8 Hrs**
UNIT-V	
Design and Applications: Developing and building a robot, models of flexible links and joints, robotic arm – Components and structure, types of joints and workspace, design models for mechanic arms and lifting systems mutiple robots, machine interface, robots in manufacturing and non- manufacturing applications, robot cell design, selection of robot. **Laboratory Sessions/ Experimental Learning:** 1. Case Study on Robots in material handling and assembly. Human Robot Interaction **Applications:** Humanoid, Robotic Arms.	**8 Hrs**

Course Outcomes: After completing the course, the students will be able to	
CO1	Analyze the concept development and key components of robotics technologies.
CO2	Select the components for interfacing actuators.
CO3	Implement basic mathematics manipulations of spatial coordinate representation and Transformation.
CO4	Solve basic robot forward and inverse kinematic problems.
CO5	Design robots which are capable to solve basic robotic dynamics, path planning and control problems.
Text Books:	
1.	Introduction to Robotics By S.K.Saha , Tata McGraw Hill
2.	Robotics Control, Sensing, Vision and Intelligence by K.S. Fu, R.C .Gonzalez, C.S.G.Lee, Tata McGraw HillJ. Hirchhorn: Kinematics and Dynamics of Machinery, McGraw Hill book Co.
Reference Books:	
1.	Robert J. Schilling, Fundamentals of Robotics- Analysis and Control, Prentics Hall india.
2.	Robotics Technology and Flexible Automation by S.R.Deb, S. Deb, Tata McGraw Hill
3.	Robot Motion and Control (Recent Developments) by M.Thoma& M. Morari

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for

16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: IV		
DATA STRUCTURES USING PYTHON		
Course Code:	**MVJ22VL454**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40 L**	**SEE Duration: 03 Hours**

Course Learning Objectives: The students will be able to

1	Understand the fundamentals of data structures and their applications in logic building and project assessment.
2	Understand the concept of linked lists and sorting techniques.
3	Acquire the knowledge of algorithms of queues and stacks.
4	Analyze the concepts of binary trees.
5	Examine Graphs and its algorithms.

UNIT-I	
Python Primer: Python Overview, Objects in Python, Expressions, Operators, Control Flow, Functions, Simple i/p and o/p, Modules. **Basic Concepts of Data Structures and Algorithms:** Introduction- Variables, Datatypes, Data Structures, ADT, what is an algorithm, How to compare algorithms, Rate growth, Types of analysis, Asymptotic Notation, Performance Analysis: Space complexity, Time complexity, Guidelines for asymptotic analysis. **Searching Techniques:** Linear Search and Binary Search **Laboratory Sessions/ Experimental learning**: 1. Develop a mini project to demonstrate the concept Binary Search. **Applications:** The Library Management System can be deployed in small libraries to: Manage Book Inventory, Register Members, Search Efficiently	**8 Hrs**
UNIT-II	
Linked Lists: Definition, Linked list operations: Traversing, Searching, Insertion, and Deletion. Doubly Linked lists and its operations, Circular linked lists and its operations. **Sorting Techniques:** Bubble Sort, Insertion Sort, Selection Sort, Quick Sort and Merge Sort.	**8 Hrs**

Laboratory Sessions/ Experimental learning: **1.** Develop an algorithm to demonstrate the concept of Linked lists. **Applications:** Student Management System using linked lists and sorting techniques to manage student records, including traversing, searching, inserting, and deleting records.	
UNIT-III	
Stacks: Definition, Stack Implementation using arrays/lists and linked lists, Stack ADT, Stack Operations (Insertion and Deletion), Array Representation of Stacks, Stack Applications: Infix to postfix conversion, Tower of Hanoi. **Queues:** Definition, Array Representation, Queue Implementation using arrays/lists and linked lists, Queue ADT, Operations on queues (Insertion and Deletion), Circular Queues and its operations, Priority Queues and its operations. **Laboratory Sessions/ Experimental learning:** 1. Implementation of Towers of Hanoi using Stacks. **Applications:** An Expression Evaluation and Task Scheduling System using stacks and queues to manage and evaluate arithmetic expressions, as well as to schedule and manage tasks.	**8 Hrs**
UNIT-IV	
Trees: Terminology, Binary Trees, Types of Binary trees, Properties of Binary trees, Array Representation of Binary Trees, Binary Tree Traversals – Inorder, Postorder, Preorder. Binary Search Trees – Definition, Insertion, Deletion, Searching, Implementation of Binary tree, Heaps and Heap Sort, Construction of Expression Trees, AVL Trees. **Laboratory Sessions/ Experimental learning:** 1. Solve Parenthesis Matching problem using binary search trees. **Applications:** A Task Management System to manage and organize tasks using various tree data structures. This system will allow users to add, delete, and search for tasks, as well as sort tasks based on their priorities using heaps.	**8 Hrs**
UNIT-V	
Graphs: Definitions, Terminologies, Matrix and Adjacency List Representation of Graphs, Elementary Graph operations, Traversal methods: Breadth First Search and Depth	**8 Hrs**

First Search, DAG, Minimum Spanning Trees: Prim – Kruskal algorithm, Single Source Shortest Path: Weighted graphs, Dijkstra algorithm. **Laboratory Sessions/ Experimental learning:** 1. Print all the nodes of graph using DFS and BFS. 2. Apply various algorithms on a graph and analyse it. Applications: Use DAGs to represent scenarios where relationships have a direction and there are no cycles, such as task scheduling.	

Course Outcomes: After completing the course, the students will be able to	
CO1	Acquire knowledge of Python fundamentals and data structures.
CO2	Analyse and design of algorithms for Linked lists and sorting techniques.
CO3	Apply the concepts of Stacks and queues.
CO4	Utilize the operations of search trees and their applications.
CO5	Investigate Graphical algorithms.
Text Books:	
1.	Rance D Necaise "Data Structures and Algorithms using Python", Wiley, John Wiley and Sons.
2.	Michael T. Goodrich, R. Tamassia and Michael H Goldwasser "Data structures and Algorithms in python", Wiley student edition, John Wiley and Sons.
Reference Books:	
1.	Narasimha Karumanchi, "Data Structures and Algorithmic Thinking with Python", CareerMonk Publications.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are

20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: III		
ANALOG ELECTRONICS		
Course Code:	**MVJ22VL32**	**CIE Marks:100**
Credits:	**L:T:P: 3:0:2**	**SEE Marks: 100**
Hours:	**40L+26P**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Understand low frequency response for various configurations of BJT and FET amplifier.	
2	Understand the different topologies of feedback amplifiers and oscillators.	
3	Analyze the power amplifier circuits in different modes of operation.	
4	Analyze typical frequency response graphs for each of the filter circuits and switching circuits of Op-Amps.	
5	Compare various types of DACs and ADCs, timer IC's and evaluate the performance of each with neat circuit diagrams.	

UNIT 1	
Prerequisites: *Operation of PN junction diode* **P-N Junction Diode**: Load line analysis, diode applications - Limiters, clippers, clampers, voltage multipliers, half wave & full wave rectification. **Special Purpose Diodes** - Zener diode, varactor diode, light emitting diodes, laser diodes. **Laboratory Sessions/ Experimental Learning:** 1. Construct and analyze a full-wave rectifier **Video Link/ Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/105/108105158/	**8Hrs.**
UNIT 2	
Prerequisites: *Working of BJT.* **Bipolar Junction Transistors (BJT):** Introduction, DC operating point, fixed bias, emitter bias with and without emitter resistance, voltage divider bias, dc bias with voltage feedback, analysis of above circuits and their design, variation of operating point and its stability.	**8Hrs.**

Laboratory Sessions/ Experimental Learning: 1. Plot the transfer and drain characteristics of a BJT and calculate its drain resistance, mutual conductance and amplification factor. **Video Link/ Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/105/108105158/	
UNIT 3	
Transistors Amplifier: Small signal BJT amplifiers: AC equivalent circuit, hybrid, re model and their use in amplifier design. Multistage amplifiers, frequency response of basic & compound configuration. **Laboratory Sessions/ Experimental Learning:** 1. Plot the frequency response using any class of power amplifier. **Video Link/ Additional Online Information:** 1. http://www.nptelvideos.in/2012/12/electronics.html	**8Hrs.**
UNIT 4	
OP-Amps and its Applications: Ideal Op-Amp, practical op-amp circuits, differential and common mode operation, inverting & non inverting amplifier, integrator, differentiator, summing, scaling and averaging amplifiers, buffer, instrumentation amplifier, Schmitt Trigger **Active Filters**: First and second order low-pass and high-pass Butterworth filters, band-pass filters, band reject filters. **Laboratory Sessions/ Experimental Learning:** 1. Design and test the voltage-shunt feedback amplifier and calculate the parameters using with and without feedback. 2. Design and find the gain of a differential amplifier. **Video Link/ Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/105/108105158/	**8Hrs.**

UNIT 5	
Feedback Circuits: Effect of positive and negative feedbacks, basic feedback topologies & their properties, Analysis of practical feedback amplifiers. **Oscillators:** Oscillator operation, FET based phase shift oscillator, Wien bridge oscillator, LC and crystal oscillators. **555 Timer and its Applications:** Mono-stable and astable multivibrators. **Laboratory Sessions/ Experimental Learning:** 1. Construct a Wien Bridge Oscillator circuit using an operational amplifier and analyse the output waveform. **Video Link/ Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/105/108105158/	**8Hrs.**

Course Outcomes: After completing the course, the students will be able to	
CO1	Explain the principles of analog electronic circuits, describing device characteristics such as transistor operation modes, biasing techniques, and small-signal models.
CO2	Apply knowledge of analog circuit analysis to design and simulate basic amplifier circuits, filters, and oscillators.
CO3	Analyze the performance of analog circuits by evaluating frequency response, gain-bandwidth product, and stability criteria.
CO4	Design analog integrated circuits (ICs) by integrating transistor-level designs into functional blocks such as operational amplifiers (op-amps).
CO5	Lab

LIST OF EXPERIMENTS

S. No.	**Experiment Name**
1	Design a monostable multivibrator using 555 timer.
2	Design a astable multivibrator using 555 timer.
3	Design a RC phase shift oscillator.
4	Design a inverting Schmitt trigger.
5	Design a narrow band-pass filter and narrow band-reject filter.

6	Design a precision full-wave rectifier.
7	Input and output characteristics of transistor CB configuration
8	Input and output characteristics of transistor CE configuration

Text Books	
1.	Robert L. Boylestad and louis Nashelsky, "Electronic Devices and Circuit Theory", PHI/Pearson Education,11th Edition.
2.	Adel S Sedra, Kenneth C Smith "Microelectronic Circuits, Theory and Applications", 6th Edition, Oxford, 2015.ISBN:978-0-19-808913-1.
Reference Books	
1.	Behzad Razavi, "Fundamentals of Microelectronics", John Weily ISBN 2013 978-81-265-2307-8,2nd Edition.
2.	K.A.Navas, "Electronics Lab Manual", Volume I, PHI, 5th Edition, 2015, ISBN: 9788120351424.
3.	"Operational Amplifiers and Linear IC"s", David A. Bell, 2nd edition, PHI/Pearson. ISBN 978-81-203-2359-9.
4.	"Linear Integrated Circuits", D. Roy Choudhury and Shail B. Jain, 4th edition, New Age International ISBN 978-81-224-3098-1.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks

adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

Laboratory- 50 Marks

Experiment Conduction with proper results is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**1**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO2	**3**	**3**	**1**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**1**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**1**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**1**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: III		
PHYSICS OF SEMICONDUCTOR DEVICES		
Course Code:	**MVJ22VL33**	**CIE Marks: 50**
Credits:	**L:T:P: 3:0:2**	**SEE Marks: 50**
Hours:	**40L+26P**	**SEE Duration: 3 Hrs**

Course Learning Objectives: The students will be able to	
1	Understand the fundamentals of intrinsic, extrinsic semiconductors with carrier concentration.
2	Analyze the current-voltage characteristics of a diode.
3	Analyze the performance and behavior of semiconductor devices under different operating conditions by examining capacitance-voltage (C-V) profiles.
4	Analyze various short channel effects in MOSFET.
5	Distinguish between different types of diodes and their characteristics.

UNIT 1	
Semiconductor Fundamentals: Crystal structure, quantum mechanics, energy bands and charge carriers in solids, Fermi level, carrier concentration in semiconductors, intrinsic and extrinsic semiconductors, density of states, Fermi distribution, equilibrium concentration, Boltzmann statistics, direct and indirect band-gap. **Carrier Transport in Semiconductors:** Current flow mechanisms: Drift current, diffusion current, mobility of carriers, current density equations, continuity equation. **Laboratory Sessions/ Experimental Learning:** 1. Measure and compare the resistivity of intrinsic and extrinsic (doped) semiconductors **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/108/108108122/	**8Hrs.**
UNIT 2	
P-N Junction: Energy band diagrams, space charge layers, poisson equation, electric fields and potentials, p-n junction under applied bias, static current-voltage characteristics of p-n junctions, breakdown mechanisms (Avalanche breakdown, Zener process), Reverse bias junction capacitance.	**8Hrs.**

Laboratory Sessions/ Experimental Learning: 1. Observe the current-voltage behavior of a diode in forward and reverse bias **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/108/108108122/	
UNIT 3	
Metal Semiconductor Contact: Ideal MS contact, ohmic contact, rectifying contact, schottky diode. **MOS Capacitor:** Ideal MOS fundamentals**,** accumulation, depletion and inversion, threshold voltage, factors affecting the threshold voltage, CV characteristics of ideal MOS. **Laboratory Sessions/ Experimental Learning:** 1. Measure the gate capacitance of MOSCAP and understand its variation with applied voltage. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/108/108108122/	**8Hrs.**
UNIT 4	
Non Ideal MOS: Metal semiconductor work function difference**,** oxide charges: Mobile ions, fixed charges, interfacial traps, induce charges, CV characteristics of non-ideal MOS. **MOSFETs:** Theory of operation, I_D-V_D characteristics, I_D-V_G characteristics, Scaling and Short Channel Effects, drain-induced barrier lowering, velocity saturation, impact ionization, Channel length modulation, Hot carrier effect. **Laboratory Sessions/ Experimental Learning:** 1. Measure the I_D –V_D at various gate voltage for n channel MOSFET. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/108/108108122/	**8Hrs.**

UNIT 5	
Modern FET Structures: FinFETs, structure and design of FinFET, benefits over Planar MOSFETs, SOI (Silicon on insulator) MOSFET, GAAFETs (Gate-All-Around FETs). **Laboratory Sessions/ Experimental Learning:** 1. Measure the I-V characteristics and efficiency of a SOI MOSFET. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/108/108108122/	**8Hrs.**

Course Outcomes: After completing the course, the students will be able to	
CO1	Explain the band structure diagrams of intrinsic and extrinsic semiconductors.
CO2	Solve the electrostatics of PN junction diode and draw its characteristics in positive and negative bias.
CO3	Analyze the fundamentals parameters of MOS capacitor.
CO4	Analyze the MOSFET in various regimes (linear, cut off and saturation)
CO5	Distinguish various III-V semiconductor devices. (Lab)
LIST OF EXPERIMENTS	
S. No.	**Experiment Name**
1.	To study the I-V characteristics of a PN junction diode and understand its behaviour under forward and reverse bias conditions.
2.	To examine the I-V characteristics of an n-channel MOSFET.
3.	To understand its operation in different regions (cut off, linear, and saturation).
4.	To study the electrical characteristics of light emitting diodes (LEDs)
5.	To analyze the I-V characteristics of a solar cell and determine its efficiency and fill factor.
6.	To analyse zener diode characteristics and show zener diode as a voltage regulator
7.	
8.	
Text Books:	

1.	Semiconductor Device Fundamentals" by Robert F. Pierret, Addison-Wesley, ISBN: 0-201-54393-1
2.	Streetman, B. and Banerjee, S., Solid State Electronics, Prentice Hall India.
Reference Books:	
1.	Sze, S.M., Physics of Semiconductor Devices, John Wiley.
2.	Advanced Semiconductor Fundamentals" by Robert F. Pierret, Addison-Wesley, ISBN: 0-201-54393-1

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

Laboratory- 50 Marks

Experiment Conduction with proper results is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

CO-PO-PSO Mapping													
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**1**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO2	**3**	**3**	**1**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**1**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**1**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**1**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: III		
ANALYSIS AND DESIGN OF DIGITAL CIRCUITS		
Course Code:	**MVJ22VL34**	**CIE Marks:50**
Credits:	**L:T:P:S 3:0:0:Y**	**SEE Marks: 50**
Hours:	**40 L**	**SEE Duration: 03 Hours**

Course Learning Objectives: The students will be able to

1	Explain the basic principles of digital logic design, including the operation of logic gates, flip-flops, and the distinction between combinational and sequential circuits.
2	Interpret Boolean expressions and demonstrate the use of truth tables and Karnaugh maps in simplifying logical expressions for combinational circuits.
3	Apply digital design principles to construct basic combinational circuits.
4	Design sequential circuits, such as counters and shift registers, by utilizing flip-flops.
5	Design digital systems using programmable logic devices (PLDs).

UNIT-I

Prerequisites: *Number systems, Boolean Algebra, Logic Gates, Comparison of Combinational & Sequential Circuits.* **Principles of Combinational Logic**: Introduction, canonical forms, generation of switching equations from truth tables, Karnaugh maps-3, 4 variables, incompletely specified functions (Don't care terms), Quine- McClusky techniques- 3 & 4 variables. **Laboratory Sessions/ Experimental Learning**: 1. Study of Logic Gates – NOT, OR, AND, NOR, NAND, XOR and XNOR. 2. Design a 4-bit Binary to Gray code converter using logic gates. **Applications:** OR gate in detecting exceed of threshold values and producing command signal for the system and AND gate in frequency measurement. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc21_ee10/preview	**8 Hrs**

UNIT-II

***Prerequisites*: *Decoder, Encoders, Multiplexers & Demultiplexer*.** **Design and Analysis of Combinational Logic:** Half adder & subtractor, full adder & subtractors, parallel adder and subtractor, look ahead carry adder, BCD adder, binary comparators, multiplexers and demultiplexers, decoders, encoders, priority encoder **Laboratory Sessions/ Experimental Learning:** 1. Design a full adder with two half adders using logic gates. 2. Design an Adder cum Subtractor circuit which adds when input bit operation=1 or subtract if 0, using logic gates. 3. Design 4-bit comparator using IC7485. 4. Realize a Boolean expression using decoder IC74139. **Applications:** Communication systems, speed synchronization of multiple motors in industries. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc21_ee10/preview	**8 Hrs**
UNIT-III	
Prerequisites*: *SR, JK, D, T flipflops **Flip-Flops and Its Applications:** Latches and flip flops, master-slave JK flip-flop, timing concerns in sequential circuits, shift registers – SISO, SIPO, PISO PIPO, universal shift register, counters – synchronous and asynchronous. **Laboratory Sessions/ Experimental Learning:** 1. Develop SR, D, JK &T flip flop using logic gates 2. Design a 6-bit Register using D-Flipflop **Applications:** Frequency divider circuit, frequency counter. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc21_ee10/preview	**8 Hrs**
UNIT-IV	
Sequential Circuit Design: Characteristic equations, design of a synchronous mod-n counter using clocked JK, D, T and SR flip-flops, Melay & Moore models, design of a sequence detector.	**8 Hrs**

Laboratory Sessions/ Experimental Learning: 1. Design a synchronous counter for a given sequence- 0, 2, 4, 6, 0 2. Design a 4-bit asynchronous up/down counter 3. Design a 4-bit binary synchronous up/down **Applications:** Data synchronizer, counter. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc21_ee10/preview	
UNIT-V	
Memory Devices: Basic memory structure: ROM, PROM, EPROM, EEPROM, RAM- Static and dynamic RAM Programmable Logic Devices: Programmable Logic Array (PLA), Programmable Array Logic (PAL), Field Programmable Gate Arrays (FPGA), Implementation of combinational logic circuits using PLA, PAL. **Laboratory Sessions/ Experimental Learning:** 1. Designing of combinational logic circuits using PLA, PAL. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc21_ee10/preview	**8 Hrs**

Course Outcomes: After completing the course, the students will be able to	
CO1	Describe the algebraic equations using K-map & Quine-McCluskey technique.
CO2	Explain the operation and characteristics of fundamental digital electronic components, including logic gates, flip-flops, and multiplexers, and describe their roles in digital circuits.
CO3	Interpret and construct truth tables and Boolean expressions for various digital logic circuits.
CO4	Apply digital design techniques to develop combinational and sequential circuits.
CO5	Analyze and design finite state machines (FSMs) by evaluating state transition diagrams, constructing state tables, and designing sequential circuits using FSMs.
Text Books:	

1.	Morris Mano, ―Digital Design , Prentice Hall of India, Third Edition.
2.	John M Yarbrough, "Digital Logic Applications and Design", Thomson Learning.
Reference Books:	
1.	Charles H Roth Jr., Larry L. Kinney ―Fundamentals of Logic Design, CengageLearning 7th Edition.
2.	Donald D. Givone, "Digital Principles and Design", McGraw Hill.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: III		
DIGITAL CIRCUIT LABORATORY		
Course Code:	**MVJ22VLL35**	**CIE Marks: 50**
Credits:	**L:T:P:0:0:2**	**SEE Marks: 50**
Hours:	**26P**	**SEE Duration: 3 Hrs**

Course Learning Objectives: The students will be able to	
1	Understand digital logic levels and application of knowledge to further understand digital electronics circuits.
2	Analyze the design of various digital electronic circuits.
3	Apply the knowledge of digital circuits and systems to efficiently, reliably, and economically to achieve desired results.
4	Execute the techniques for modelling and troubleshooting circuits and systems through structural and gate-level networks and breadboard designs.
5	Analyze the timing diagrams of digital circuits to understand their temporal behavior.

LIST OF EXPERIMENTS	
S. No.	**Experiment Name**
1	To study and verify truth table of logic gates
2	To realize half/full adder and half/full subtractor
3	To realize IC7483 as parallel adder/subtractor
4	To verify BCD to excess 3-code conversion using NAND gates. To study and verify the truth table of excess-3 to BCD code convertor
5	To convert given binary numbers to gray code.
6	To verify truth table of MUX and DEMUX using NAND
7	To verify the truth table of one bit and two bit comparators using logic gates
8	To convert a given octal input to binary output and to study the LED display using 7447 7-segment decoder
9	To verify the truth table of flipflops
10	To design bi-synchronous counter using T-flipflop
Course Outcomes: After completing the course, the students will be able to	

CO1	Understand the fundamental concepts and techniques used in digital electronics.
CO2	Identify and describe the functions of various digital components.
CO3	Solve boolean functions using logic gates.
CO4	Describe the truth tables of different combinational & sequential circuits.
CO5	Analyze the performance and behavior of digital circuits.

CO-PO-PSO Mapping														
CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
CO1	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**3**	**-**	**-**	2	**1**	**1**
CO2	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**3**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**3**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**3**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**3**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: III		
PRINCIPLES OF COMMUNICATION		
Course Code:	**MVJ22VL361**	**CIE Marks:50**
Credits:	**L:T:P 3:0:0**	**SEE Marks: 50**
Hours:	**40 L**	**SEE Duration: 03 Hours**

Course Learning Objectives: The students will be able to

1	Explain the fundamental principles of analog and digital communication systems, including modulation techniques, signal transmission, and reception.
2	Apply modulation and demodulation techniques to design analog communication systems.
3	Analyze the performance of digital communication systems by evaluating parameters such as bit error rate (BER), signal-to-noise ratio (SNR), and bandwidth efficiency.
4	Implement digital modulation schemes such as pulse code modulation (PCM), and quadrature amplitude modulation (QAM).
5	Apply the basic concepts of coherent and non-coherent digital modulation techniques and understand the basics of spread spectrum modulation.

UNIT-I

Introduction: Basic block diagram of communication system, Need of Modulation, types of modulation **Amplitude Modulation:** Introduction to AM, time-domain description, frequency-domain description, single-tone modulation, generation of AM wave: Square law modulator, switching modulator, detection of AM waves: Envelope detector **Double Side Band Suppressed Carrier (DSBSC) and SSB Modulation:** Time-domain description and frequency-domain representation **Laboratory Sessions/ Experimental Learning:** 1. Generation of AM signal using MATLAB. 2. Generation of DSBSC signal using transistor. **Applications:** Broadcast transmissions, Air band radio, Quadrature amplitude modulation. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117/105/117105143/	**8 Hrs**

UNIT-II	
Angle Modulation: Basic concepts of Phase Modulation, Frequency Modulation: Narrow band FM, wide band FM, and generation of FM waves: Indirect FM and direct FM. Detection of FM Signal: Balanced slope detector, Phase locked loop, Comparison of FM and AM., Concept of Pre-emphasis and de-emphasis. **Laboratory Sessions/ Experimental Learning:** 1. Generation of FM signal using MATLAB **Applications:** FM radio broadcasting, telemetry, radar, seismic prospecting, and monitoring new-born for seizures via EEG, two-way radio systems, sound synthesis, magnetic tape- recording systems and some video-transmission systems. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117/105/117105143/	**8 Hrs**
UNIT-III	
Transmitters: Classification of Transmitters, AM Transmitters, FM Transmitters **Receivers**: Radio Receiver - Receiver Types - Tuned radio frequency receiver, Super heterodyne receiver, RF section and Characteristics - Frequency changing and tracking, Intermediate frequency, Image frequency, AGC, Amplitude limiting, FM Receiver, Comparison of AM and FM Receivers. **Laboratory Sessions/ Experimental Learning:** 1. Investigate the effects of noise on analog modulation signals and explore noise reduction techniques. **Applications:** Biomedical engineering, communication system. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117/105/117105077/ 2. https://nptel.ac.in/courses/117/101/117101051/	**8 Hrs**
UNIT-IV	

Pulse Modulation: Types of Pulse modulation- PAM, PWM and PPM. Comparison of FDM and TDM Pulse Code Modulation: PCM Generation and Reconstruction, Quantization Noise, Non-Uniform Quantization and Companding, DPCM, Adaptive DPCM, DM and Adaptive DM, Noise in PCM and DM. **Laboratory Sessions/ Experimental Learning:** 1. Eye diagram using MATLAB **Applications:** Ethernet, RFID marker localization signals, Radar Systems **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117/105/117105077/ 2. https://nptel.ac.in/courses/117/101/117101051/	**8 Hrs**
UNIT-V	
Digital Modulation Techniques: ASK- Modulator, Coherent ASK Detector, FSK- Modulator, Non-Coherent FSK Detector, BPSK- Modulator, Coherent BPSK Detection. Principles of QPSK, Differential PSK and QAM. **Laboratory Sessions/ Experimental Learning:** 1. Analyze constellation of 16-QAM Using MATLAB **Applications:** CDMA, WiMAX (16d, 16e), telemetry, caller ID, garage door openers, wireless communication, mobile communication and satellite communication, LANs, Bluetooth, RFID, GPS, Wi-Fi, etc. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117/105/117105077/ 2. https://nptel.ac.in/courses/117/101/117101051/ 3. https://nptel.ac.in/courses/117/105/117105136/	**8 Hrs**

Course Outcomes: After completing the course, the students will be able to

CO1	Explain the concepts of analog modulation techniques such as amplitude, modulations and its variations like DSB-SC and SSB-SC.
CO2	Analyze frequency modulation and compute performance of different types of noise.
CO3	Apply the concepts of noise in analog modulation and analysis of pre-emphasis and de-emphasis circuit.
CO4	Analyze the signal space representation of digital signals.
CO5	Analyze the performance of a baseband and pass band digital communication system and spread spectrum techniques.
Text Books:	
1.	Simon Haykins & Moher, Communication Systems, 5th Edition, John Wiley, India Pvt. Ltd, 2010, ISBN 978 – 81 – 265 – 2151 – 7.
2.	Simon Haykins, "An Introduction to Analog and Digital Communication", John Wiley
Reference Books:	
1.	B P Lathi and Zhi Ding, Modern Digital and Analog Communication Systems, Oxford University Press., 4th edition, 2010, ISBN: 97801980738002.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub

divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: III		
ARTIFICIAL INTELLIGENCE AND MACHINE LEARNING		
Course Code:	**MVJ22VL362**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**

Course Learning Objectives: The students will be able to	
1	Understand the AI foundations and applications.
2	Apply machine learning algorithms to analyze and interpret real-world datasets.
3	Solve problems by searching.
4	Analyze advanced problem solving paradigms and knowledge representation.
5	Implement various learning algorithms, such as backpropagation and gradient descent, to optimize neural network parameters.

UNIT 1	
Introduction: What is artificial intelligence? What Is AI? The Foundations of Artificial Intelligence, The History of Artificial Intelligence, The State of the Art. **Heuristic Search Techniques:** Generate and test, Hill Climbing, Best First Search, Problem Reduction, Constraint Satisfaction, Means-ends Analysis. **Laboratory Sessions/ Experimental Learning:** 1. Find the shortest path from a start node to a goal node in a maze using heuristic search technique. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/106102220	**8Hrs.**
UNIT 2	
Knowledge Representation: Knowledge representation issues, predicate logic, representation knowledge using rules. **Concept Learning:** Concept learning task, concept learning as search, find-S algorithm, candidate elimination algorithm, inductive bias of candidate elimination algorithm**.**	**8Hrs.**

Laboratory Sessions/ Experimental Learning: 1. Apply the concept learning paradigm in machine learning, specifically using the Find-S algorithm to identify the most specific hypothesis from a given dataset. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/106102220	
UNIT 3	
Decision Tree Learning: Introduction, decision tree representation, appropriate problems, ID3 algorithm. **Artificial Neural Network:** Introduction, NN representation, appropriate problems, perceptrons, backpropagation algorithm. **Laboratory Sessions/ Experimental Learning:** 1. Apply decision tree representation in machine learning by building and visualizing a decision tree classifier. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/106102220	**8Hrs.**
UNIT 4	
Bayesian Learning: Introduction, Bayes theorem, Bayes theorem and concept learning, ML and LS error hypothesis, ML for predicting, MDL principle, Bates optimal classifier, Gibbs algorithm, Navie Bayes classifier, BBN, EM Algorithm **Laboratory Sessions/ Experimental Learning:** 1. Apply the concept of least squares error hypothesis in machine learning, specifically using linear regression to predict outcomes based on input features. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/106102220	**8Hrs.**
UNIT 5	

Instance-Base Learning: Introduction, k-nearest neighbour learning, locally weighted regression, radial basis function, case-based reasoning, reinforcement learning: Introduction, learning task, Q-learning. **Laboratory Sessions/ Experimental Learning:** 1. Apply the K-nearest neighbors (KNN) algorithm in machine learning, using it to classify a dataset and evaluate its performance **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/106102220	**8Hrs.**

Course Outcomes: After completing the course, the students will be able to	
CO1	Understand the fundamental principles of artificial intelligence and machine learning.
CO2	Apply machine learning algorithms such as linear regression, decision trees, to develop and train models using real-world datasets.
CO3	Implement techniques for data preprocessing to prepare datasets for machine learning tasks.
CO4	Apply the knowledge of searching and reasoning techniques for different applications.
CO5	Analyze the performance of neural network models by evaluating metrics such as accuracy, loss, precision.

Text Books:	
1.	Tom M Mitchell, “Machine Learning”, 1st Edition, McGraw Hill Education, 2017.
2.	Elaine Rich, Kevin K and S B Nair, “Artificial Intelligence”, 3rd Edition, McGraw Hill Education, 2017.
Reference Books:	
1.	Saroj Kaushik, Artificial Intelligence, Cengage learning.
2.	Stuart Rusell, Peter Norving, Artificial Intelligence: A Modern Approach, Pearson Education 2nd Edition.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
CO1	**3**	**3**	**3**	**2**	**-**	**1**	**-**	**-**	**1**	**-**	**-**	**1**	**2**	**1**
CO2	**3**	**3**	**3**	**2**	**-**	**1**	**-**	**-**	**1**	**-**	**-**	**1**	**2**	**1**
CO3	**3**	**3**	**3**	**2**	**-**	**1**	**-**	**-**	**1**	**-**	**-**	**1**	**2**	**1**
CO4	**3**	**3**	**3**	**2**	**-**	**1**	**-**	**-**	**1**	**-**	**-**	**1**	**2**	**1**
CO5	**3**	**3**	**3**	**2**	**-**	**1**	**-**	**-**	**1**	**-**	**-**	**1**	**2**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: III		
COMPUTER ORGANIZATION & ARCHITECTURE		
Course Code:	**MVJ22VL363**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**

Course Learning Objectives: The students will be able to

1	Explain the basic sub-systems of a computer, their organization, structure and operation.
2	Apply knowledge of instruction set architectures to design and implement basic assembly language programs for different processor architectures.
3	Analyze the performance of computer systems by examining factors such as pipelining, caching strategies, and parallelism.
4	Describe memory hierarchy and concept of virtual memory.
5	Analyze the design and operation of memory systems by evaluating cache coherence protocols, memory mapping techniques, and virtual memory management strategies.

UNIT 1	
Basic Structure of Computers: Computer types, functional units, basic operational concepts, bus structures, software, performance – processor clock, basic performance equation. **Machine Instructions and Programs:** Numbers, arithmetic operations and characters, IEEE standard for floating point numbers, memory location and addresses, memory operations, instructions and instruction sequencing. **Laboratory Sessions/ Experimental Learning:** 1. Understanding various parts of CPU of a PC. 2. Study of microprocessor and understanding of its various instruction **Applications:** Understand the functionality of the various units of computer. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/106/105/106105163/	**8Hrs.**
UNIT 2	
Prerequisite: *Number systems*	**8Hrs.**

Addressing Modes: Assembly language, basic input and output operations, stacks and queues, subroutines, additional instructions. **Laboratory Sessions/ Experimental Learning:** 1. Write an ALP to find the sum of two numbers and verify if the sum is an even or odd number and simulate the output. 2. Write an ALP to transfer a block of data from one location to other and simulate the output. **Applications:** Project based on microprocessor. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/106/105/106105163/	
UNIT 3	
Input/Output Organization: Accessing I/O devices, interrupts – interrupt hardware, enabling and disabling interrupts, handling multiple devices, controlling device requests, direct memory access, and buses. **Laboratory Sessions/ Experimental Learning:** Study any one input/output device and examine its various input output ports details. **Applications:** Interfacing of peripheral devices **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/106/105/106105163/	**8Hrs.**
UNIT 4	
Memory System: Basic concepts, semiconductor RAM memories- Internal organization of memory chips, static memories, asynchronous DRAMS, read only memories, cache memories, mapping functions, replacement algorithm, virtual memories, secondary storage-magnetic hard disks. **Laboratory Sessions/ Experimental Learning:** Implement and simulate a simple memory unit which is capable of reading and writing data within a single clock cycle. **Applications:** Understanding the various memories. **Video Link / Additional Online Information:**	**8Hrs.**

1. https://archive.nptel.ac.in/courses/106/105/106105163/	
UNIT 5	
Basic Processing Unit: Some fundamental concepts, execution of a complete instruction, multiple bus organization, hardwired control, micro programmed control, pipelining, basic concepts, role of cache memory, pipeline performance. **Laboratory Sessions/ Experimental Learning:** Evaluate the possible control sequence for implementing a multiplication instruction using registers for a single bus organization **Applications:** Microprocessor. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/106/105/106105163/	**8Hrs.**

Course Outcomes: After completing the course, the students will be able to	
CO1	Identify the functional units of the processor and the factors affecting the performance of a computer.
CO2	Demonstrate the ability to classify the addressing modes, instructions sets and design programs.
CO3	Understand the different ways of accessing an input / output device including interrupts.
CO4	Analyze the organization of different types of semiconductor and other secondary storage memories.
CO5	Analyze the simple processor organization based on hardwired control and micro programmed control.

Text Books:	
1.	Carl Hamacher, ZvonkoVranesic, SafwatZaky: “Computer Organization”, 6th Edition, Tata McGraw Hill, 2011.
Reference Books:	
1.	Andrew S. Tanenbaum, Todd Austin, “Structured Computer Organization”, 6th Edition, Pearson, 2013.
2.	David A. Patterson, John L. Hennessy: “Computer Organization and Design – The Hardware / Software Interface ARM Edition”, 4th Edition, Elsevier.
3.	William Stallings: “Computer Organization & Architecture”, 7th Edition, PHI.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
CO1	**3**	**3**	**3**	**2**	**-**	**1**	**-**	**-**	**1**	**-**	**-**	**1**	**2**	**1**
CO2	**3**	**3**	**3**	**2**	**-**	**1**	**-**	**-**	**1**	**-**	**-**	**1**	**2**	**1**
CO3	**3**	**3**	**3**	**2**	**-**	**1**	**-**	**-**	**1**	**-**	**-**	**1**	**2**	**1**
CO4	**3**	**3**	**3**	**2**	**-**	**1**	**-**	**-**	**1**	**-**	**-**	**1**	**2**	**1**
CO5	**3**	**3**	**3**	**2**	**-**	**1**	**-**	**-**	**1**	**-**	**-**	**1**	**2**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: III		
SENSOR TECHNOLOGY		
Course Code:	**MVJ22VL364**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Understand various technologies associated in manufacturing of sensors.	
2	Provide better familiarity with different sensors and their applications in real life.	
3	Acquire knowledge about types of sensors used in modern digital systems.	
4	Evaluate the technological and physical limitations of a specific sensor.	
5	Propose a suitable sensor for a given measurement situation.	

UNIT 1	
Prerequisite: *Basic Electronics, Knowledge on physical quantities.* **Sensors Fundamentals and Characteristics:** General concepts and terminology, sensor classification, static characteristics, dynamic characteristics, materials for sensors, microsensor technology. **Laboratory Sessions/ Experimental Learning:** **Applications:** **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/108/105/108105064/ 2. https://nptel.ac.in/courses/108/108/108108147/	**8Hrs.**
UNIT 2	
Temperature Sensors: Basic Concepts, temperature scale, standard temperature points, thermistor sensors, thermocouple sensors, pyrometer, radiation thermometer, Temperature sensor applications **Position Measurement Sensors:** Principle of position measurement, inductive sensors, capacitive sensors, capacitive and inductive sensor applications, mutual sensors, hall sensors	**8Hrs.**

Laboratory Sessions/ Experimental Learning: **Applications:** **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/108/105/108105064/ 2. https://nptel.ac.in/courses/108/106/108106165/	
UNIT 3	
Strain Gauge Sensors: Transfiguration and measurement methods, resistive metal probe, piezoresistive silicon sensors **Pressure Measurement Sensors:** Pressure measurement principles, types of pressure sensors, piezoelectric sensors, magnetoresistive sensors, characteristics of pressure sensors, pressure measurement sensor applications **Laboratory Sessions/ Experimental Learning:** **Applications:** **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/108/105/108105064/	**8Hrs.**
UNIT 4	
Optical Sensors: Luminescent sensors, photoresistors, photoelectric cells, classification of optical sensors **Fluid-flow Measurement sensors:** Flow measurement methods, types of sensors used to measure fluid flows, level sensors, flow measurement by pressure difference **Laboratory Sessions/ Experimental Learning:** 1. **Applications:** **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/108/105/108105064/	**8Hrs.**
UNIT 5	

Motion Sensors: Resistive potentiometer, LVDT, Eddy current sensor, Piezoelectric accelerator sensor **Proximity sensors:** Introduction, inductive proximity sensors, capacitive proximity sensors, optical proximity sensors, ultrasonic proximity sensors **Laboratory Sessions/ Experimental Learning:** **Applications:** **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/108/105/108105064/ 2. https://nptel.ac.in/courses/112/103/112103174/	**8Hrs.**

Course Outcomes: After completing the course, the students will be able to	
CO1	Understand the concept of sensors and its characteristics.
CO2	Explain the working principles of primary and resistive sensors.
CO3	Understand the inductive, capacitive and Electromagnetic sensors and its applications.
CO4	Identify alternative methods to measure common quantities such as temperature, pressure, force and acceleration.
CO5	Select appropriate sensors used for various applications.

Text Books:	
1.	Ramon Pallas & John G.Webster, "Sensors and signal conditioning", John Wiley & Sons., 2nd Edition.
2.	J. Fraden, "Handbook of Modern Sensors: Physical, Designs, and Applications", AIP Press, Springer, 3rd Edition
Reference Books:	
1.	D. Patranabis, "Sensors and Transducers", PHI Publication, 2nd Edition, New Delhi.
2.	Webster John G, "Instrumentation and sensors Handbook", CRC Press, 1st Edition.
3.	Shawhney A.K., "Electrical and Electronics Measurements and Instrumentation", Dhanpat Rai & Sons.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
CO1	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: IV		
FPGA BASED SYSTEM DESIGN USING VERILOG HDL		
Course Code:	**MVJ22VL41**	**CIE Marks:100**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 100**
Hours:	**40L**	**SEE Duration: 3 Hrs**

Course Learning Objectives: The students will be able to	
1	Explain the fundamental concepts of FPGA architecture, describing the components such as logic cells, interconnect resources, and configurable I/O blocks that constitute an FPGA.
2	Apply Verilog HDL to implement digital circuits on FPGA platforms.
3	Analyze the impact of design choices on FPGA resource usage and power consumption by examining synthesis reports, power analysis tools, and performance profiling.
4	Develop proficiency in writing synthesizable Verilog code for combinational and sequential logic.
5	Model designs using IP-based methodologies and tools.

UNIT 1	
Introduction to Programmable Logic Devices: Introduction to programmable logic and comparison with full custom, semi-custom, and gate array design flow. **CPLD:** Working principle, architecture, I/O block, macrocells, programming, features, examples. **FPGA:** Working principle, architecture, I/O block, CLB, embedded memory, clock management, DSP capability, programming, features, examples, FPGA design flow, prototyping solution, need for hardware description languages and implementation and verifications of digital logics on FPGA platform to prove FPGA design flow. Distinguish between HDL based digital logic design and test-bench for verifications. **Laboratory Sessions/ Experimental Learning:** 1. Understand the basics of PLDs, including their architecture and use in digital logic design. **Video Link / Additional Online Information:**	**8Hrs.**

1. https://archive.nptel.ac.in/courses/106/105/106105165/ 2. https://onlinecourses.nptel.ac.in/noc24_cs61/preview	
UNIT 2	
Verilog HDL Language: Importance and popularity of verilog HDL, typical design flow. Hierarchical modeling concepts: Top to bottom and bottom to top. Difference between design and test-bench writing using verilog, **Lexical Conventions:** Whitespace, comments, operators, number specifications, string, identifiers, keywords. **Data Types:** Value set, nets, registers, vectors, integer, real, and time register data, arrays, memories, parameters and string. System tasks and compiler directives, module, ports, and hierarchical names. **Laboratory Sessions/ Experimental Learning:** 1. Create simple verilog modules to demonstrate the use of verilog data types. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/106/105/106105165/ 2. https://onlinecourses.nptel.ac.in/noc24_cs61/preview	**8Hrs.**
UNIT 3	
Design Modeling Techniques: Gate/Structural level modeling: Highlights of structural description, organization of structural description, half adder and full adder design using structural description, half subtractor and full subtractor design using structural description. **Data Flow Level Modeling:** Highlights of data-flow description, signal declaration and assignment statement, constant declaration and constant assignment statements, assigning a delay time to the signal-assignment statement. **Behavioral Level Modeling:** Behavioral description highlights, structure of the verilog behavioral description, sequential statements: If statement, the case statement, verilog casex and casez, the wait-for statement, the loop statement: for-loop, while-loop, repeat, forever. **Switching Level Modeling:** Highlights of switching level description, MOS, CMOS switches, NOR and NAND gate implementation using switching flow. Tasks and Functions, timing and delays, modular test benches	**8Hrs.**

Laboratory Sessions/ Experimental Learning: 1. Design a 4-bit arithmetic logic unit (ALU) using behavioral modeling. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/106/105/106105165/ 2. https://onlinecourses.nptel.ac.in/noc24_cs61/preview	
UNIT 4	
Synthesis Basics: Highlights of synthesis, synthesis information from module, mapping always in the hardware domain, mapping the signal-assignment statement to gate level, mapping logical operators, mapping the IF statement, mapping the case statement, mapping the loop statement. **Implementation:** Mapping, placement and routing. **Laboratory Sessions/ Experimental Learning:** 1. Analyze the synthesis report to understand the resource utilization and timing summary. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/106/105/106105165/ 2. https://onlinecourses.nptel.ac.in/noc24_cs61/preview	**8Hrs.**
UNIT 5	
IP-Based Digital Logic Design And Logic Validation: Basics of AXI interfacing, IP-based counter implementation, IP-based different clock generator, FIFO, and BRAM. **Real Time Logic Validations:** Integrated logic analyzer (Xilinx ILA IP) and virtual input and output (VIO). **Laboratory Sessions/ Experimental Learning:** 1. Analyze timing diagrams and understand the signaling involved in AXI transactions. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc24_cs61/preview	**8Hrs.**

Course Outcomes: After completing the course, the students will be able to	
CO1	Explain the basic architecture and functioning of FPGAs.
CO2	Develop synthesizable Verilog HDL code for combinational and sequential logic circuits.
CO3	Make use of simulation tools to debug and validate Verilog HDL code.
CO4	Understand the FPGA design flow, including synthesis, placement, and routing.
CO5	Develop AXI-based interfaces for high-speed communication within FPGA designs.

Text Books	
1.	Palnitkar, S. "Verilog HDL: A guide to Digital Design and Synthesis" 2nd ed. Pearson.
2.	Sass, Ronald, and Andrew G. Schmidt, "Embedded systems design with platform FPGAs: Principles and practices", Morgan Kaufmann.
Reference Books	
1.	J. A Bhasker, "System Verilog Primer" 1st Indian ed. B.S. Publication.
2.	Steve Kilts, Advanced FPGA design: architecture, implementation, and optimization" John Wiley & Sons.
3.	Pong P Chu, "FPGA prototyping by Verilog examples: Xilinx Spartan-3 version" John Wiley & Sons.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**
CO2	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**
CO3	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**
CO4	**3**	**2**	**2**	**-**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**
CO5	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: IV		
NETWORK THEORY		
Course Code:	**MVJ22VL42**	**CIE Marks: 50**
Credits:	**L: T:P: 3:0:2**	**SEE Marks: 50**
Hours:	**40L+26P**	**SEE Duration: 3 Hrs.**

Course Learning Objectives: The students will be able to	
1	Understand the basic network concepts emphasizing source transformation, mesh and nodal techniques to solve for resistance/impedance, voltage, current and power.
2	Apply Thevenin's, Millman's, superposition, reciprocity, maximum power transfer and Norton's Theorems in solving the problems related to electrical circuits.
3	Analyze the frequency response of series and parallel combination of passive components as resonating circuits.
4	Describe the behavior of RLC circuits in the time and frequency domain.
5	Analyze the two port network parameters like Z, Y, T and h and their inter-relationships.

UNIT-I	
Ohm's law, Kirchhoff's laws **Basic Concepts:** Introduction, practical sources, source transformations, star – delta transformation, loop and node analysis with linearly dependent and independent sources for DC networks, concepts of super node and super mesh. **Laboratory Sessions/ Experimental Learning:** 1. Find the current through and voltage across the load in the circuit. **Applications:** Simplification and analysis of analog circuits, microwave circuit analysis. **Video Link /Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/105/108105159/	**8 Hrs**
UNIT-II	
Graph Theory and Network Equations: Graph of a network, trees, co-trees and loops, incidence matrix, cut-set matrix, tie-set matrix and loop currents, number of possible trees of a graph, analysis of networks, duality.	**8 Hrs**

Laboratory Sessions/ Experimental Learning: 1. Understand and apply graph theory concepts such as trees, co-trees, loops, incidence matrices, cut-set matrices, tie-set matrices, and loop currents to the analysis of electrical networks. **Applications:** Simplification and analysis of analog circuits, microwave circuit analysis. **Video Link /Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/105/108105159/	
UNIT-III	
Network Theorems: Superposition theorem, Millman's theorem, Thevenin's and Norton's theorems, reciprocity theorem, maximum power transfer theorem. **Laboratory Sessions/ Experimental Learning**: 1. Verify superposition theorem for a circuit. **Applications:** Simplification and analysis of analog circuits, microwave circuit analysis. **Video Link /Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/105/108105159/	**8 Hrs**
UNIT-IV	
Prerequisites: *Laplace Transforms, Properties of Laplace Transform and Inverse Laplace Transform using partial fraction method.* **Transient Behaviour and Initial Conditions:** Behaviour of circuit elements under switching condition and their representation, evaluation of initial and final conditions in RL, RC and RLC circuits for DC excitations, applications of Laplace transforms in circuit analysis. **Laboratory Sessions/ Experimental Learning:** 1. Plot the response of a series RLC circuit. **Applications:** In the analysis of transmission lines and waveguides. **Video Link /Additional Online Information:** **1.** https://archive.nptel.ac.in/courses/108/105/108105159/	**8 Hrs**

UNIT-V	
Two Port Network Parameters: Introduction, open circuit impedance parameter, short circuit admittance parameter, hybrid parameters, transmission parameter, relationship between parameters. **Laboratory Sessions/ Experimental Learning:** 1. Plot the frequency response characteristics for a series RL, RC circuit. 2. Plot the frequency response characteristics for a parallel RL circuit. 3. Measure two port parameters for a given network **Applications:** For analysis of communication systems and antennas. **Video Link /Additional Online Information:** **1.** https://archive.nptel.ac.in/courses/108/105/108105159/	**8 Hrs**

Course Outcomes: After completing the course, the students will be able to	
CO1	Apply network simplification techniques to calculate currents and voltages in a circuit.
CO2	Describe the network problems using graphical methods.
CO3	Apply network theorems to simplify the complex circuits.
CO4	Examine and differentiate between transient and steady-state responses of electrical circuits to various inputs, using techniques such as differential equations and Laplace transforms.
CO5	Analyze the given network using specified two port network parameters like Z or Y or T or h and evaluate the frequency response related parameters through the RLC elements, in resonant circuits. (Lab)

LIST OF EXPERIMENTS

S. No.	**Experiment Name**
1.	Apply the kirchoff's law for finding current in a complex electrical circuit.
2.	Verification of Norton and maximum power transfer theorems in ac circuits.
3.	Apply the Thevenin theorem for finding current in a complex electrical circuit.
4.	Determination of transient response of current in RL and RC circuits with step voltage input.

5.	Determination of transient response of current in RLC circuit with step voltage input for under damp, critically damp and over damp cases.
6.	To determine the equivalent parameters of series connection of two port network.
7.	
8.	

Text Books	
1.	M.E. Van Valkenberg, "Network analysis", Prentice Hall of India, 3rd edition, ISBN: 9780136110958.
2.	Roy Choudhury, "Networks and systems", 2nd edition, New Age International Publications, ISBN: 9788122427677.
Reference Books	
1.	Hayt, Kemmerly and Durbin ―Engineering Circuit Analysis", TMH 7th Edition, 2010.
2.	J. David Irwin /R. Mark Nelms, "Basic Engineering Circuit Analysis", John Wiley, 8th edition.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

Laboratory- 50 Marks

Experiment Conduction with proper results is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

Semester: IV		
ELECTROMAGNETIC FIELD THEORY		
Course Code:	**MVJ22VL43**	**CIE Marks:50**
Credits:	**L:T:P:S 3:0:0:Y**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Understand the physical significance of Biot-Savart's Law, Amperes' circuital law and Stokes' theorem for different current distributions.	
2	Apply mathematical methods, including vector calculus and differential equations, to solve problems related to electromagnetic fields.	
3	Analyze electromagnetic wave propagation by evaluating wave equations, polarization states, and propagation characteristics in different media.	
4	Understand the concepts of Smith Chart for impedance matching.	
5	Analyze the interaction between electromagnetic fields and materials by examining concepts such as dielectric and magnetic properties.	

UNIT 1	
Prerequisites: *Vector algebra, coordinate systems (Rectangular coordinate system, cylindrical coordinate system and spherical coordinate system), gradient, divergence and curl.* **Electrostatics: Coulomb's Law, Electric Field Intensity, Flux Density And Potential:** Coulomb's law, electric field intensity, field due to line charge, field due to Sheet of charge, field due to continuous volume charge distribution, electric flux, electric flux density, electric potential, potential difference, relation between electric field intensity (E) & potential (V), potential gradient, electric dipole, energy density in electrostatic fields. **Laboratory Sessions/ Experimental Learning:** 1. Determine the electric field intensity at a point due to uniform linear charge (ρ L) and point charges using MATLAB. 2. Determine the electric field intensity at a point due to surface charge using MATLAB.	**8 Hrs.**

3. Determine the potential difference between two points on a ring having linear charge density, ρ L using MATLAB. **Applications:** The Van de Graaff generator, Xerography, Ink Jet Printers and Electrostatic Painting, Smoke Precipitators and Electrostatic Air Cleaning. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/104/108104087/	
UNIT 2	
Gauss' law, Divergence, Poisson's and Laplace's Equations: Gauss law, Maxwell's first equation, application of Gauss' law, divergence theorem, current, current density, conductor, the continuity equation, boundary conditions (dielectric-dielectric, conductor-dielectric, conductor-free space), Poisson's and Laplace's equations. **Laboratory Sessions/ Experimental Learning:** 1. Evaluate the current flowing through a given surface using MATLAB. 2. Verify the divergence theorem using MATLAB. **Applications:** Used for calculation electrical field for a symmetrical distribution of charges. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/104/108104087/	**8 Hrs.**
UNIT 3	
Magnetostatics: Steady magnetic field-Biot-Savart law, Ampere's circuital law, Curl, Stokes' theorem, Gauss's law for magnetic fields, magnetic flux and magnetic flux density, Maxwell's equations for static fields, magnetic scalar and vector Potentials. **Magnetic Forces And Magnetic Materials:** Force on a moving charge and differential current element, force between differential current elements, magnetization, magnetic susceptibility, permeability, magnetic boundary conditions, inductances, magnetic energy, magnetic circuit. **Laboratory Sessions/ Experimental Learning:** 1. Determine the magnetic field intensity at a point due to magnetic field using MATLAB. **Applications:** Motors, Generators, Loudspeakers, MRI. **Video Link / Additional Online Information:**	**8 Hrs.**

1. https://archive.nptel.ac.in/courses/108/104/108104087/	
UNIT 4	
Time Varying Fields and Electromagnetic Wave Propagation: Time varying fields & Maxwell's equations, Faraday's law, transformer and motional electro - motive forces, displacement current, Maxwell's equation in differential and integral form, time varying potentials. **Electromagnetic Wave Propagation:** Derivation of wave equations from Maxwell's equations, relation between E and H, Wave propagation in - lossy dielectrics, lossless dielectrics, free space and good conductor, skin-effect, Poynting theorem. **Laboratory Sessions/ Experimental Learning:** 1. Determine the parameters of wave using MATLAB. **Applications:** Optoelectronics. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/104/108104087/	**8 Hrs.**
UNIT 5	
Transmission Line: Introduction, transmission line parameters, transmission line equations, input impedance, standing wave ratio and power, Smith Chart basic fundamentals, types of transmission lines - coaxial line, strip line, micro strip line. **Applications of Transmission Line**: Impedance matching and tuning: Single stub tuning, double stub tuning, and the quarter wave transformer. **Laboratory Sessions/ Experimental Learning:** 1. Simulation of micro strip transmission line using FEKO software. **Applications:** Telephone, Cable TV, Broadband network **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/104/108104087/	**8 Hrs.**
Course Outcomes: After completing the course, the students will be able to	

CO1	Solve problems on electrostatic force, electric field due to point, linear, surface charge and volume charges.
CO2	Apply Gauss law to evaluate electric fields due to different charge distributions by using Divergence Theorem.
CO3	Apply Biot-Savart's and Ampere's laws for evaluating magnetic field for different current configurations.
CO4	Apply Maxwell's equations for time varying fields and evaluate power associated with EM waves using Poynting theorem.
CO5	Design electromagnetic devices and systems, such as antennas and transmission lines, while optimizing performance characteristics such as impedance matching and radiation patterns.

Text Books:	
1.	Matthew N. O. Sadiku, "Elements of Electromagnetics", Oxford University Press, Edition VII, 2018.
2.	David M Pozar, "Microwave Engineering", John Wiley & Sons, Inc., 4th edition, 2014.
Reference Books:	
1.	W.H. Hayt. J.A. Buck & M Jaleel Akhtar, "Engineering Electromagnetics", Tata McGraw – Hill, Edition VIII, 2014.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: IV		
VERILOG HDL LABORATORY		
Course Code:	**MVJ22VLL44**	**CIE Marks: 50**
Credits:	**L:T:P:0:0:2**	**SEE Marks: 50**
Hours:	**26P**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Understand architectures of FPGA , CPLD and different IC design flow.	
2	Apply verilog HDL design flow and hierarchical modeling to design various digital circuits.	
3	Design and verify circuits using various verilog modeling techniques.	
4	Grasp the synthesis process from high-level design to hardware implementation.	
5	Implement and validate designs using IP-based methodologies and tools.	

LABORATORY SESSIONS	
PART A	
Exp. No	**Experiment Name**
1.	Write Verilog program for the following combinational logic, verify the design using test bench and perform the synthesis by downloading the design on to FPGA device. a. Structural modeling of Full adder using two half adders and or Gate b. BCD to Excess-3 code converter
2.	Write Verilog program for the following Sequential Circuits, verify the design using test bench and perform the synthesis by downloading the design on to FPGA device. a. Mod-N counter b. Random sequence counter
3.	Write Verilog program for the following Sequential Circuits, verify the design using test bench and perform the synthesis by downloading the design on to FPGA device. a. SISO and PISO shift register b. 4-Bit Linear Feedback shift register b. Barrel Shifter

4.	Write Verilog program for the following Digital Circuits, verify the functionality using test bench and perform the synthesis by downloading the design on to FPGA device. a. Ring Counter b. Johnson Counter
5.	Write Verilog program for the following Digital Circuits, verify the functionality using test bench and perform the synthesis by downloading the design on to FPGA device. a. 4-Bit Ripple Carry Adder b. 4-bit Array Multiplication. c. 4-bit Booth Multiplication
PART B	
6	Write a Verilog code to design a clock divider circuit that generates 1/2, 1/3rdand 1/4thclock from a given input clock. Port the design to FPGA and validate the Functionality through ILA.
7	Generate 3 different clock frequencies using predefined IP and validate using oscilloscopes.
8	Write a Verilog code to interface LED and display HDL on the LED display and also validate all output using VIO IP before implementations
9	Design a FSM to detect 1010 patterns and validate real time detection of patterns using ILA IP
10	Write Verilog code to convert an analog input of a sensor to digital form by interfacing ADC to display the same on a suitable display like set of simple LEDs like 7-Segment display digits.
11	Interface a DAC to FPGA and write Verilog code to generate Square wave of Frequency F KHz. Modify the code to down sample the frequency to F/2 KHz. Display the original and Down sampled signals by connecting them to an Oscilloscope.
Course Outcomes: After completing the course, the students will be able to	
CO1	Develop proficiency in writing Verilog code for modelling digital systems at various levels of abstraction (behavioral, dataflow, and structural).

CO2	Apply Verilog HDL to design and simulate basic digital circuits such as logic gates, multiplexers, and flip-flops, using simulation tools to verify circuit functionality.
CO3	Analyze the behavior of Verilog-based designs by evaluating simulation results, identifying and debugging errors in the Verilog code, and optimizing designs for performance.
CO4	Design and implement complex digital systems, such as finite state machines (FSMs)
CO5	Implement Verilog designs on Field-Programmable Gate Arrays (FPGAs) and understand the FPGA design flow.

CO-PO-PSO Mapping														
CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
CO1	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**
CO2	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**
CO3	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**
CO4	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**
CO5	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**

High-3, Medium-2, Low-1

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B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: IV		
CONTROL SYSTEMS		
Course Code:	**MVJ22VL451**	**CIE Marks:100**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 100**
Hours:	**40L**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Explain the fundamental principles and components of control systems.	
2	Apply control theory to model dynamic systems using differential equations and state-space representations.	
3	Analyse the response of first and second order systems using standard test signals and analyse steady state error.	
4	Analyse stability of systems using RH criteria, root locus, Nyquist, Bode plot and polar plot.	
5	Design controllers such as PID, lead-lag, and state feedback controllers to achieve desired system performance specifications.	

UNIT 1	
Introduction to Control Systems: Open loop and closed loop systems, types of feedback, differential equation of physical systems – Mechanical systems, electrical systems, analogous systems. **Block Diagrams and Signal Flow Graphs:** Transfer functions, block diagram algebra and signal flow graphs. **Laboratory Sessions/ Experimental Learning:** 1. Determine and plot poles and zeros from the transfer function using MATLAB. **Applications:** Electric hand drier, automatic washing machine, DC motor, automatic electric iron, voltage stabilizer**.** **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/107/106/107106081/	**8Hrs.**
UNIT 2	

Time Response of Feedback Control Systems: Standard test signals, unit step response of first and second order systems. Time response specifications of first order systems, time response specifications of second order systems for underdamped system, steady state errors and error constants. **Introduction to Controllers:** P, PI, PD and PID Controllers. **Laboratory Sessions/ Experimental Learning:** 1. Obtain step and impulse response of a unity feedback first order system for a given forward path transfer function using MATLAB. 2. Obtain step and impulse response of a unity feedback second order system for a given forward path transfer function using MATLAB. **Applications:** Industrial control systems **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/107/106/107106081/	**8Hrs.**
UNIT 3	
Stability Analysis Using RH Criteria And Root Locus: Concepts of stability, necessary conditions for stability, Routh Hurwitz stability criterion, relative stability analysis, introduction to root-locus techniques, the root locus concepts, construction of root loci. **Laboratory Sessions/ Experimental Learning:** 1. Obtain root locus plot of the system for a given forward path transfer function using MATLAB. **Applications:** Used to determine the dynamic response of a s system. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/107/106/107106081/	**8Hrs.**
UNIT 4	
Stability Analysis using Nyquist Criteria and Bode Plots: Polar plot, Nyquist stability criterion, Nyquist plots, Bode plots, gain and phase margin. **Laboratory Sessions/ Experimental Learning:** 1. Obtain Bode plot of the system for a given forward path transfer function using MATLAB.	**8Hrs.**

2. Obtain Nyquist plot of the system for a given forward path transfer function using MATLAB. **Applications:** To determine a stability of a system. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/107/106/107106081/	
UNIT 5	
Introduction to State Variable Analysis: Concepts of state, state variable and state models for electrical systems, solution of state equations, state transition matrix and its properties. lag, lead and lag lead compensation. **Laboratory Sessions/ Experimental Learning:** 1. Determining the solution of state equations using MATLAB. **Applications:** State variables are used to describe the future response of a d+ynamic response. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/107/106/107106081/	**8Hrs.**

Course Outcomes: After completing the course, the students will be able to	
CO1	Apply mathematical models to represent and simulate the behavior of dynamic systems.
CO2	Analyze transient and steady state response of second order systems using standard test signals and analyze steady state error.
CO3	Analyze the stability of the systems by applying RH criteria and root locus techniques.
CO4	Analyze the stability of the system using frequency domain techniques such as Nyquist and Bode plots.
CO5	Design and implement controllers, such as proportional-integral-derivative (PID) controllers, lead-lag compensators, and state feedback controllers.

Text Books:	
1.	Nagarath and M.Gopal, Control Systems Engineering, New Age International (P) Limited, Publishers, Fifth edition, ISBN: 81-224-2008.

2.	Modern Control Engineering, K.Ogata, Pearson Education Asia/PHI, 4th Edition, ISBN 978-81-203-4010-7.
Reference Books:	
1.	Automatic Control Systems‖, Benjamin C. Kuo, John Wiley India Pvt. Ltd., 8th Edition.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping

CO/ PO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
CO1	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: IV		
INDUSTRIAL ELECTRONICS		
Course Code:	**MVJ22VL452**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40 L**	**SEE Duration: 03 Hours**

Course Learning Objectives: The students will be able to

1	Explain broad types of industrial power devices, there structure, and its characteristics.
2	Design and analyse the broad categories of power electronic circuits.
3	Explain various types of MEMs devices, principle of operation and construction.
4	Familiarize with soft core processors and computer architecture
5	Apply protective methods for devices and circuits.

UNIT-I

Industrial Power Devices: General purpose power diodes, fast recovery power diodes, schottky power diodes, silicon carbide power diodes, Power MOSFETs, Steady state characteristics, switching characteristics, silicon carbide MOSFETs, COOLMOS, Junction field effect transistors, operation and characteristics of JFETs, Silicon Carbide JFET structures, Bipolar Junction Transistors, Steady state characteristics, switching characteristics, silicon carbide BJTs, IGBT, silicon carbide IGBTs **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/105/108105063/	**8 Hrs**

UNIT-II

Power Electronics Circuits: Thyristor, Thyristor characteristics, two transistor model. Controlled Rectifiers – Single phase full converter with R and RL load, Single phase dual converters, and Three phase full converter with RL load. Switching mode regulators – Buck Regulator, Boost regulator, Buck – Boost regulator, comparison of regulators **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/105/108105063/	**8 Hrs**

UNIT-III	
Inverters – Principle of operation, Single phase bridge inverter, Three phase inverter with 180 and 120 degree conduction, Current source inverter. AC voltage controllers – Single phase full wave controller with resistive load, single phase full wave controller with inductive load **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/105/108105063/	**8 Hrs**
UNIT-IV	
MEMS Devices: Sensing and Measuring Principles, Capacitive Sensing, Resistive Sensing, Piezoelectric Sensing, Thermal Transducers, Optical Sensors, Magnetic Sensors, MEMS Actuation Principles, Electrostatic Actuation, Thermal Actuation, Piezoelectric Actuation, Magnetic Actuation, MEMS Devices Inertial Sensors, Pressure Sensors, Radio Frequency MEMS: Capacitive Switches and Phase Shifters, Microfluidic Components, Optical Devices. **MEMS Applications:** Introduction, Industrial, Automotive, Biomedical **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/105/108105063/	**8 Hrs**
UNIT-V	
Protections of Devices and Circuits: Cooling and Heat sinks, Thermal Modeling of Power Switching Devices, Electrical Equivalent Thermal model, Mathematical Thermal Equivalent Circuit, Coupling of Electrical and Thermal Components, Snubber circuits, Voltage protection by Selenium Diodes and Metaloxide Varistors, Current protection, Fusing, Fault current with AC source, Fault current with DC source, Electromagnetic Interference, sources of EMI, Minimizing EMI Generation, EMI shielding, EMI standards **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/105/108105063/	**8 Hrs**

Course Outcomes: After completing the course, the students will be able to

CO1	Explain different types of industrial power devices such as MOSFET, BJT, IGBT etc, there structure, and its operating characteristics.
CO2	Design and analyse the power electronic circuits such as switch mode regulators, inverters, controlled rectifiers and ac voltage controllers.
CO3	Explain various types of MEMs devices used for sensing pressure, temperature, current, voltage, humidity, vibration etc..
CO4	Familiarize with soft core processors such as ASIC and FPGA.
CO5	Familiarize with computer hardware, software, architecture, instruction set, memory organization, multiprocessor architecture.
Text Books:	
1.	Power Electronics: Devices, Circuits, and Applications, Muhammad H. Rashid, Pearson, 4th International edition.
2.	Fundamentals of Industrial Electronics , Bogdan M. Wilamowski, J. David Irwin, CRC Press.
Reference Books:	
1.	Thomas E. Kissell, Industrial Electronics: Applications for Programmable Controllers, Instrumentation and Process Control, and Electrical Machines and Motor Controls, 3rd edition, Prentice Hall.
2.	Ned Mohan, T.M. Undeland and W.P. Robbins, “Power Electronics: Converters, Applications and Design”, Wiley India Ltd.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: IV		
ROBOTICS AND AUTOMATION		
Course Code:	**MVJ22VL453**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40 L**	**SEE Duration: 03 Hours**

Course Learning Objectives: The students will be able to

1	Explain the fundamental concepts and principles of robotics and automation.
2	Apply mathematical and computational techniques to model robotic mechanisms.
3	Analyze the performance and efficiency of robotic systems by evaluating parameters such as accuracy, repeatability, and speed.
4	Analyze basic robotic dynamics, path planning and control problems.
5	Design and implement control algorithms for robotic systems.

UNIT-I

Basic Concepts In Robotics: Definition, anatomy of robot, basic structure of robot, specifications and classification of robot, safety measures in robotics, industrial applications of robots. Drives for robots: Electric, hydraulic and pneumatic. Sensors: Internal-external, contact-non-contact, position, velocity, force, torque, proximity and range. **Laboratory Sessions/ Experimental Learning:** 1. Interface various sensors with Microcontroller. **Applications:** Machine Tending**,** Picking, Packing and Palletizing, painting, all Industrial applications. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/112/105/112105249/ 2. https://nptel.ac.in/courses/112/101/112101098/	**8 Hrs**

UNIT-II

Robot Drivers, Sensors And Vision: Introduction to techniques, image acquisition and processing, different types of grippers- Mechanical, magnetics, vacuum, adhesive, gripper force analysis and gripper design, overview of actuators, power and torque, acceleration and velocity specifications and characteristics of stepper motors, AC motors, DC motors and servomotors. **Laboratory Sessions/ Experimental Learning:** 1. Interface motors using various motor drivers. **Applications:** Industrial application, agriculture robots, surgical robots. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/112/105/112105249/ 2. https://nptel.ac.in/courses/112/101/112101098/	**8 Hrs**
UNIT-III	
Robot Kinematics And Dynamics: Direct and inverse kinematics for industrial robots for position and orientation, redundancy, manipulator, direct and inverse velocity. Link inertia tensor and manipulator inertia tensor, Newton–Eller formulation for RP and RP manipulators, trajectory planning. **Laboratory Sessions/ Experimental Learning:** 1. Interface servo motors to form gripper. **Applications:** Pick and Place, Excavators, Robotic ARM. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/112/105/112105249/ 2. https://nptel.ac.in/courses/112/101/112101098/	**8 Hrs**
UNIT-IV	
Robot Kinematics: Dynamics and programming methods, robot language classification, robot language structure, kinematics and path planning: Solution of inverse kinematics problem, multiple solution jacobian work envelop, hill climbing techniques, robot programming languages elements and its functions. Simple programs on sensing distance and direction, Line following algorithms, feedback systems.	**8 Hrs**

Laboratory Sessions/ Experimental Learning: 1. Design algorithm for Maze solving robot. **Applications:** Defence, Surveillance, Autonomous Vehicle. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/112/105/112105249/ 2. https://nptel.ac.in/courses/112/101/112101098/	
UNIT-V	
Design and Applications: Developing and building a robot, models of flexible links and joints, robotic arm – Components and structure, types of joints and workspace, design models for mechanic arms and lifting systems mutiple robots, machine interface, robots in manufacturing and non- manufacturing applications, robot cell design, selection of robot. **Laboratory Sessions/ Experimental Learning:** 1. Case Study on Robots in material handling and assembly. Human Robot Interaction **Applications:** Humanoid, Robotic Arms. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/112/105/112105249/ 2. https://nptel.ac.in/courses/112/101/112101098/	**8 Hrs**

Course Outcomes: After completing the course, the students will be able to	
CO1	Analyze the concept development and key components of robotics technologies.
CO2	Select the components for interfacing actuators.
CO3	Implement basic mathematics manipulations of spatial coordinate representation and Transformation.
CO4	Solve basic robot forward and inverse kinematic problems.
CO5	Design robots which are capable to solve basic robotic dynamics, path planning and control problems.
Text Books:	

1.	Introduction to Robotics By S.K.Saha , Tata McGraw Hill
2.	Robotics Control, Sensing, Vision and Intelligence by K.S. Fu, R.C .Gonzalez, C.S.G.Lee, Tata McGraw HillJ. Hirchhorn: Kinematics and Dynamics of Machinery, McGraw Hill book Co.
Reference Books:	
1.	Robert J. Schilling, Fundamentals of Robotics- Analysis and Control, Prentics Hall india.
2.	Robotics Technology and Flexible Automation by S.R.Deb, S. Deb, Tata McGraw Hill
3.	Robot Motion and Control (Recent Developments) by M.Thoma& M. Morari

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**

CO4	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: IV		
DATA STRUCTURES USING PYTHON		
Course Code:	**MVJ22VL454**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40 L**	**SEE Duration: 03 Hours**

Course Learning Objectives: The students will be able to

1	Understand the fundamentals of data structures and their applications in logic building and project assessment.
2	Understand the concept of linked lists and sorting techniques.
3	Acquire the knowledge of algorithms of queues and stacks.
4	Analyze the concepts of binary trees.
5	Examine Graphs and its algorithms.

UNIT-I

Python Primer: Python Overview, Objects in Python, Expressions, Operators, Control Flow, Functions, Simple i/p and o/p, Modules. **Basic Concepts of Data Structures and Algorithms:** Introduction- Variables, Datatypes, Data Structures, ADT, what is an algorithm, How to compare algorithms, Rate growth, Types of analysis, Asymptotic Notation, Performance Analysis: Space complexity, Time complexity, Guidelines for asymptotic analysis. **Searching Techniques:** Linear Search and Binary Search Applications: developing computational tools and bioinformatics software, Mathematics. **Laboratory Sessions/ Experimental learning**: 1. Develop a mini project to demonstrate the concept Binary Search. **Video link / Additional online information:** 1. http://www.nptelvideos.com/video.php?id=1442 2 2. https://nptel.ac.in/courses/106105085/	**8 Hrs**

UNIT-II

Prerequisites: Programming using the concept of Arrays and pointers	**8 Hrs**

Linked Lists: Definition, Linked list operations: Traversing, Searching, Insertion, and Deletion. Doubly Linked lists and its operations, Circular linked lists and its operations. **Sorting Techniques:** Bubble Sort, Insertion Sort, Selection Sort, Quick Sort and Merge Sort. **Laboratory Sessions/ Experimental learning:** **1.** Develop an algorithm to demonstrate the concept of Linked lists. **Video link / Additional online information:** 1. https://nptel.ac.in/courses/106/102/106102064/	
UNIT-III	
Stacks: Definition, Stack Implementation using arrays/lists and linked lists, Stack ADT, Stack Operations (Insertion and Deletion), Array Representation of Stacks, Stack Applications: Infix to postfix conversion, Tower of Hanoi. **Queues:** Definition, Array Representation, Queue Implementation using arrays/lists and linked lists, Queue ADT, Operations on queues (Insertion and Deletion), Circular Queues and its operations, Priority Queues and its operations. **Laboratory Sessions/ Experimental learning:** 1. Implementation of Towers of Hanoi using Stacks. **Video link / Additional online information:** 1 .https://nptel.ac.in/courses/106/106/106106127/	**8 Hrs**
UNIT-IV	
Trees: Terminology, Binary Trees, Types of Binary trees, Properties of Binary trees, Array Representation of Binary Trees, Binary Tree Traversals – Inorder, Postorder, Preorder. Binary Search Trees – Definition, Insertion, Deletion, Searching, Implementation of Binary tree, Heaps and Heap Sort, Construction of Expression Trees, AVL Trees. **Laboratory Sessions/ Experimental learning:** 1. Solve Parenthesis Matching problem using binary search trees. **Video link / Additional online information:** 2. https://nptel.ac.in/courses/106/106/106106127/ 3. https://nptel.ac.in/courses/106/105/106105225/	**8 Hrs**

UNIT-V	
Graphs: Definitions, Terminologies, Matrix and Adjacency List Representation of Graphs, Elementary Graph operations, Traversal methods: Breadth First Search and Depth First Search, DAG, Minimum Spanning Trees: Prim – Kruskal algorithm, Single Source Shortest Path: Weighted graphs, Dijkstra algorithm. **Laboratory Sessions/ Experimental learning:** 1. Print all the nodes of graph using DFS and BFS. 2. Apply various algorithms on a graph and analyse it. **Video link / Additional online information:** 1. https://nptel.ac.in/courses/106/106/106106133/	**8 Hrs**

Course Outcomes: After completing the course, the students will be able to	
CO1	Acquire knowledge of Python fundamentals and data structures.
CO2	Analyse and design of algorithms for Linked lists and sorting techniques.
CO3	Apply the concepts of Stacks and queues.
CO4	Utilize the operations of search trees and their applications.
CO5	Investigate Graphical algorithms.
Text Books:	
1.	Rance D Necaise “Data Structures and Algorithms using Python”, Wiley, John Wiley and Sons.
2.	Michael T. Goodrich, R. Tamassia and Michael H Goldwasser “Data structures and Algorithms in python”, Wiley student edition, John Wiley and Sons.
Reference Books:	
1.	Narasimha Karumanchi, “Data Structures and Algorithmic Thinking with Python”, CareerMonk Publications.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may

be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

B. E. (VLSI DESIGN AND TECHNOLOGY)

Semester: V		
ARM MICROCONTROLLER AND EMBEDDED SYSTEMS		
Course Code:	**MVJ22VL52**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:2**	**SEE Marks: 50**
Hours:	**40L+26P**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Explain the architecture and core components of ARM microcontrollers.	
2	Describe the basic principles of embedded systems design, including real-time constraints, power management, and interfacing with external devices.	
3	Develop and debug embedded applications using ARM microcontrollers.	
4	Implement interfacing techniques for connecting ARM microcontrollers to peripheral devices.	
5	Implement real-time operating system (RTOS) concepts on ARM microcontrollers.	

UNIT 1	
Microprocessors Versus Microcontrollers, ARM Embedded Systems: The RISC design philosophy, The ARM design philosophy, embedded system hardware, embedded system software. ARM processor fundamentals: Registers, current program status register, pipeline, exceptions, interrupts, and the vector table, core extensions **Laboratory Sessions/ Experimental Learning**: 1. Execute simple assembly programs on an ARM-based system or emulator. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc22_cs93/preview	**8Hrs.**
UNIT 2	
Introduction To The ARM Instruction Set: Data processing instructions, branch instructions, software interrupt instructions, program status register instructions, coprocessor instructions, loading constants. **ARM Programming Using Assembly Language:** Writing assembly code, profiling and	**8Hrs.**

cycle counting, instruction scheduling, register allocation, conditional execution, looping constructs. **Laboratory Sessions/ Experimental Learning**: 1. Execute assembly programs that demonstrate various instructions and their functionalities. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc22_cs93/preview	
UNIT 3	
Embedded System Components: Embedded vs general computing system, history of embedded systems, classification of embedded systems, major applications areas of embedded systems, purpose of embedded systems, Core of an embedded system including all types of processor/controller, memory, sensors, actuators, LED, 7 segment LED display, stepper motor, keyboard, push button switch, communication interface (onboard and external types), embedded firmware, other system components. **Laboratory Sessions/ Experimental Learning**: 1. Hands-on experience with various components commonly found in embedded systems by interfacing them with a microcontroller and writing simple programs to control and monitor their behavior. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc22_cs93/preview	**8Hrs.**
UNIT 4	
Embedded System Design Concepts: Characteristics and quality attributes of embedded systems, operational quality attributes, non-operational quality attributes, embedded systems-application and domain specific, hardware software co-design and program modelling, embedded firmware design and development. **Laboratory Sessions/ Experimental Learning:**	**8Hrs.**

1. Apply fundamental concepts of embedded system design by designing, implementing, and testing a basic embedded system using a microcontroller. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc22_cs93/preview	
UNIT 5	
RTOS And IDE For Embedded System Design: Operating system basics, types of operating systems, task, process and threads (only POSIX threads with an example program), thread preemption, multiprocessing and multitasking, task communication (without any program), task synchronization issues – racing and deadlock, concept of binary and counting semaphores (mutex example without any program), how to choose an RTOS, integration and testing of embedded hardware and firmware, embedded system development environment – block diagram (excluding keil), disassembler/decompiler, simulator, emulator and debugging techniques, target hardware debugging, boundary scan **Laboratory Sessions/ Experimental Learning:** 1. Hands-on experience with a Real-Time Operating System (RTOS) and Integrated Development Environment (IDE) for embedded system design by creating and deploying a simple real-time application. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc22_cs93/preview	**8Hrs.**

Course Outcomes: After completing the course, the students will be able to	
CO1	Describe the architectural features and instructions of ARM microcontroller.
CO2	Apply the knowledge gained for programming ARM for different applications.
CO3	Analyze and optimize the performance of embedded systems based on ARM microcontrollers.
CO4	Interpret the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
CO5	Develop the hardware /software co-design and firmware design approaches.

LIST OF EXPERIMENTS	
S.No.	**Experiment Name**
1	Write a program to multiply two 16 bit binary numbers.
2	Write a program to find the sum of first 10 integer numbers.
3	Write a program to find factorial of a number.
4	Write a program to add an array of 16 bit numbers and store the 32 bit result in internal RAM
5	Write a program to find the square of a number (1 to 10) using look-up table.
6	Write a program to find the largest/smallest number in an array of 32 numbers .
7	Write a program to arrange a series of 32 bit numbers in ascending/descending order.
8	Write a program to count the number of ones and zeros in two consecutive memory locations.

Text Books:	
1.	Andrew N Sloss, Dominic Symes and Chris Wright, ARM System Developers Guide, Elsevier, Morgan Kaufman publishers.
2.	Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education, Private Limited, 2nd Edition.
Reference Books:	
1.	Steve Furber, ARM System-on-Chip Architecture, Second Edition, Pearson, 2015.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: V		
DIGITAL VLSI DESIGN		
Course Code:	**MVJ22VL53**	**CIE Marks:50**
Credits:	**L:T:P:S 4:0:0:Y**	**SEE Marks: 50**
Hours:	**40 L**	**SEE Duration: 03 Hours**

Course Learning Objectives: The students will be able to

1	Explain the basic principles and technologies used in CMOS digital integrated circuit design.
2	Utilize VLSI design techniques to create and optimize combinational circuits.
3	Design and analyze static and dynamic sequential circuits.
4	Evaluate and analyze the performance, power consumption, and reliability of various digital VLSI circuits.
5	Design and analyze various memory structures.

UNIT-I

Introduction to Digital IC Design: Digital ICs design flow, issues in digital integrated circuit design, MOS transistor basics –static and dynamic behaviour, secondary effects. CMOS inverter static and dynamic behaviour, noise margin, power consumption and power delay product, latch up, technology scaling. **Project Based Learning:** **1.** Design, simulate, and analyze a MOS transistors analyse static, dynamic behaviours with its secondary effects and also check static and dynamic power. **Laboratory Sessions/ Experimental Learning:** 1. Understand the static and dynamic behavior of a CMOS inverter through simulation and analysis. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/107/108107129/ 2. https://onlinecourses.nptel.ac.in/noc20_ee05/preview	**8 Hrs**

UNIT-II

Combinational Logic Gates: Static CMOS design: Complementary CMOS, ratioed logic, pass transistor logic. Dynamic CMOS design: basic principles, performance of dynamic logic, noise consideration, power consumption in CMOS gates – Switching activity, glitches, logical efforts, layout rules. **Project Based Learning:** 1. Design the CMOS logics Y=A+B+C and verify its dynamic and static behaviour and also evaluate the performance metrics (power, delay and cell area(Layout). **Laboratory Sessions/ Experimental Learning:** 1. Design and simulate a ratioed logic circuit to understand its behavior and performance. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/107/108107129/ 2. https://onlinecourses.nptel.ac.in/noc20_ee05/preview	**8 Hrs**
UNIT-III	
Sequential Circuits: **Static Latches and Registers:** Bistability principle, SR flip-flops, CMOS static flip-flop, multiplexer-based latches, master-slave edge-triggered register, low-voltage static latches. **Dynamic Latches and Registers:** Dynamic transmission-gate edge-triggered registers, C2MOS—A clock-skew insensitive, pulse registers, sense-amplifier based registers. **Pipelining:** Latch- vs. register-based pipelines, NORA-CMOS—A logic style for pipelined structures **Project Based Learning:** 1. Design a 4-bit register using FF and evaluate functionality, operating speed and validate their setup and hold time. Check whether hold/setup time is predefined or design dependent. **Laboratory Sessions/ Experimental Learning:** 1. Create the schematic, perform functional verification, and analyze the performance of a static flip-flop circuit. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/107/108107129/ 2. https://onlinecourses.nptel.ac.in/noc20_ee05/preview	**8 Hrs**

UNIT-IV	
Non-Bistable Sequential Circuits: The Schmitt trigger, monostable sequential circuits, astable circuits. **Datapath Subsystems:** Adder: half adder, full adder, ripple carry adder (RCA), carry-look ahead adder (CLA), carry select adders (CSL), carry skip adder, subtractor, multipliers: Booth multiplier and Wallace tree multiplier and Dadda multiplier, comparators, ring and Johnson counter barrel shifters, and generalized ALU: 1 bit ALU. **Project Based Learning:** 1. Design RCA, CLA and CSL and Carry Skip adder and do comparative study among them. **Laboratory Sessions/ Experimental Learning:** 1. Understand the design, simulation, and analysis of non-bistable sequential circuits, focusing on Schmitt trigger. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/107/108107129/ 2. https://onlinecourses.nptel.ac.in/noc20_ee05/preview	**8 Hrs**
UNIT-V	
Memories and Array Structures: ROM and RAM cells design, SRAM: Cell, array and peripheral circuits, signal to noise margin of SRAM cell, capacitance and sources of SRAM power consumption, DRAM: DRAM cells, DRAM architecture ROM: NOR and NAND ROM, FLASH and advantages and disadvantages of ROM, SRAM and DRAM. **Application:** Register, FIFO/LIFO. **Project Based Learning:** 1. Analyse the corners effects of 6T-SRAM cell and also analyse the stability of SRAM by performing HSNM, RSNM, WSNM. Learn Monte Carlo simulation check the deviation in SNMs with respect design parameters (L, W etc.) **Laboratory Sessions/ Experimental Learning:** 1. Create the schematic, perform functional verification, and analyze the performance of	**8 Hrs**

a 6T SRAM cell **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/107/108107129/ 2. https://onlinecourses.nptel.ac.in/noc20_ee05/preview	

Course outcomes: After completing the course, the students will be able to	
CO1	Understand the fundamental concepts and methodologies of digital integrated circuit (IC) design.
CO2	Analyze combinational logic gates using CMOS technology, focusing on performance metrics such as delay, power, and area.
CO3	Analyze static latches and registers, as well as dynamic latches and registers, with an emphasis on timing, stability, and power consumption.
CO4	Design and implement pipelined circuits and non-bistable sequential circuits, understanding their role in enhancing the performance and efficiency in VLSI systems.
CO5	Design and analyze datapath subsystems and memory array structures, focusing on their integration into larger VLSI systems for optimized performance.
Text Books:	
1.	J. M. Rabaey, "Digital Integrated Circuits - A Design perspective", 2nd ed. Pearson Education.
Reference Books:	
1.	Neil Weste, and K. Eshraghian, "Principles of CMOS VLSI Design - A Systems perspective", 4th Edition Addison-Wesley.
2.	S.M. Kang and Yusuf Leblebici, Chulwoo Kim "CMOS Digital Integrated Circuits, Analysis and Design" 4th Edition, McGraw Hills Publication, 2019

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated

for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: V		
VLSI LABORATORY-1		
Course Code:	**MVJ22VLL54**	**CIE Marks: 50**
Credits:	**L:T:P:0:0:2**	**SEE Marks: 50**
Hours:	**26P**	**SEE Duration: 3 Hrs**

Course Learning Objectives: The students will be able to	
1	Understand the CMOS technology, including transistor characteristics and design rules.
2	Design and implement basic digital circuits such as logic gates, multiplexers, and adders using CMOS technology.
3	Analyze voltage transfer characteristics (VTC) of digital circuits to understand static behavior and optimize for speed, power, and area.
4	Design and verify sequential circuits including static latches, dynamic registers, and flip-flops.
5	Design SRAM memory and analyze its performance in terms of stability

LABORATORY SESSIONS:	
PART A	
Exp. No	**Experiment Names**
1	Draw the CMOS schematic and Layout of the inverter circuit, and analyze voltage transfer characteristics (VTC or DC) and Dynamic characteristics (transient) to determine propagation delay, rise time fall time and also validate layout versus schematic (LVS).
2	Draw the CMOS schematic of the 2 input NAND and NOR gate, also draw the layout of the same and analyze the functions using transient analysis, in addition to that validate LVS and extract RC.
3	Draw the CMOS schematic of the Half Adder circuit and verify it with truth table, and draw the layout of the same, and simulate transient analysis to validate LVS.
4	Draw the CMOS circuit of the 4:1 Multiplexer circuit and verify it with truth table, and also draw the layout of the same and simulate transient analysis to validate LVS.

5	Draw the CMOS circuit of the 2:4 Decoder verify it with truth table, and also draw the layout of the same and simulate transient analysis to validate LVS.
PART B	
6	Draw a J-K FF and validate the design using transient analysis.
7	Design a latch based Sense Amplifier and validate the design.
8	Design a 6T-SRAM and analyse HOLD, READ and WRITE operation using transient analysis.
9	Design peripheral circuits of SRAM: Decoder, Mux, Sense-Amplifier, Pre-charge Circuits etc.
10	Design 4*4 i.e. 4 bit SRAM circuits: Analyse the circuits in terms SNM: HSNM, RSNM, WSNM.

Course Outcomes: After completing the course, the students will be able to

CO1	Demonstrate the ability to design and draw the schematic and layout of CMOS circuits, including basic gates and inverters.
CO2	Analyze voltage transfer characteristics (VTC), dynamic characteristics, and key performance metrics such as propagation delay, rise time, and fall time of digital circuits
CO3	Design, simulate, and verify various combinational logic circuits, ensuring correct functionality and optimization for performance.
CO4	Design, simulate, and analyze both static and dynamic sequential circuits, such as latches and flip-flops.
CO5	Design memory structures like SRAM cells and analyze their stability and performance.

CO-PO-PSO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**
CO2	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**
CO3	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**
CO4	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**
CO5	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: V		
VLSI FABRICATION TECHNOLOGY		
Course Code:	**MVJ22VL551**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Explain the fundamental principles and processes involved in VLSI fabrication, including lithography, deposition, etching, and doping techniques.	
2	Demonstrate proficiency in mask layout design and optimization for photolithography and mask alignment techniques.	
3	Analyze the impact of process variations and defects on VLSI device performance and yield.	
4	Evaluate the trade-offs between different fabrication techniques (e.g., CMOS vs. BiCMOS) in terms of performance, power consumption, and scalability.	
5	Critically assess the challenges and solutions in achieving nanoscale feature sizes and integration densities in modern VLSI fabrication.	

UNIT 1	
Prerequisites*: Basic science.* **Introduction to Microelectronics Fabrication And Crystal Growth:** Introduction and historical perspective, crystallography and crystal structure, crystal defects, Czochralski and float zone growth, sheet resistant measurement, Hall measurement (classification of clean room), basic fabrication process, **Laboratory Sessions/ Experimental Learning:** 1. To study the details regarding the crystal structure. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117106093	**8Hrs.**
UNIT 2	
Thermal Oxidation: Oxidation techniques: Importance of oxidation, types of oxidation techniques, growth mechanism, factors affecting the growth mechanisms, silicon oxidation model, dry & wet oxidation, Oxide charges in Si/SiO_2 system.	**8Hrs.**

Laboratory Sessions/ Experimental Learning: 1. Measure the oxide thickness grown on Si wafer grown in dry furnace. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117106093	
UNIT 3	
Lithography: Basic concepts, lithography techniques-optical lithography, electron beam lithography, x-ray lithography, ion beam lithography, photoresists, light sources and wafer exposure systems, optics, modulation transfer function **Laboratory Sessions/ Experimental Learning:** 1. Measure the minimum feature size of patterned silicon using optical microscopy. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117106093	**8Hrs.**
UNIT 4	
Diffusion: Diffusion mechanisms; diffusion reactor; diffusion profile; diffusion kinetics; parameters affecting diffusion profile; dopants and their behaviors, choice of dopants. **Ion Implantation:** Reactor design, impurity distribution profile, properties of ion implantation, low energy and high energy ion implantation. **Laboratory Sessions/ Experimental Learning:** 1. Measure the resistivity of doped area of wafer. **Video Link / Additional Online Information:** 2. https://nptel.ac.in/courses/117106093	**8Hrs.**
UNIT 5	
Deposition: Types of deposition system, thermal deposition, e-beam deposition, sputtering.	**8Hrs.**

Etching: Performance metric s of etching; types of etching- wet and dry etching; dry etching techniques-ion beam or ion-milling, sputter ion plasma etching and reactive ion etching (RIE). **CMOS technology:** Process flow. **Laboratory Sessions/ Experimental Learning:** 1. Measure the thickness of metal deposited onto the wafer. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117106093	

Course Outcomes: After completing the course, the students will be able to	
CO1	Describe the basic process flow of CMOS fabrication process.
CO2	Analyze the factor affecting the oxide growth mechanism.
CO3	Apply knowledge of VLSI fabrication principles to design and optimize mask layouts for photolithography.
CO4	Analyze the dose required for given doping in diffusion and ion implantation techniques.
CO5	Analyze the impact of advanced fabrication techniques (e.g., advanced lithography, multi-patterning) on device scaling and integration density.

Text Books:	
1.	Silicon VLSI Technology: Fundamentals, Practice and Modeling Book by Jim Plummer, Michael D. Deal, and Peter B. Griffin.
2.	The Science and Engineering of Microelectronic Fabrication by Stephen A. Campbell

Reference Books:	
1.	VLSI Fabrication Principles: Silicon and Gallium Arsenide by Sorab K. Ghandhi.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks.

Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

B. E. (VLSI DESIGN AND TECHNOLOGY)

Semester: V		
DESIGN FOR TESTABILITY		
Course Code:	**MVJ22VL552**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40 L**	**SEE Duration: 03Hours**

Course Learning Objectives: The students will be able to

1	Understand the significance and challenges of VLSI testing.
2	Apply testability techniques and structured approaches in VLSI designs.
3	Implement boundary scan (IEEE 1149.1) standards to facilitate board-level testing and debugging of integrated circuits.
4	Develop ATPG methods for combinational and sequential circuits.
5	Analyze the trade-offs between different DFT methodologies (scan design vs. BIST) in terms of area overhead, test application time, and fault coverage.

UNIT-I	
Introduction to Testing: Importance of testing, testing during the VLSI lifecycle, challenges in VLSI testing: test generation, fault models, levels of abstraction in VLSI testing, historical review of VLSI test technology: automatic test equipment, automatic test pattern generation, fault simulation, digital circuit testing, analog and mixed-signal circuit testing, design for testability, board testing, boundary scan testing. **Laboratory Sessions/ Experimental Learning:** 1. Understand and implement boundary scan testing techniques for testing and debugging printed circuit boards (PCBs). **Video link / Additional Online Information:** 1. https://archive.nptel.ac.in/noc/courses/noc16/SEM2/noc16-ec08/ 2. https://nptel.ac.in/courses/106103016	**8 Hrs**
UNIT-II	

Design for Testability: Testability Analysis: SCOAP testability analysis, probability-based testability analysis, simulation-based testability analysis, RTL testability analysis, Design for Testability Basics: *Ad Hoc* approach, structured approach, Scan Cell Designs: Muxed-D scan cell, clocked-scan cell, LSSD scan cell, Scan Architectures: Full-scan design, partial-scan design, random-access scan design Scan Design Rules: Tristate buses, bidirectional I/O ports, gated clocks, derived clocks, combinational feedback loop, asynchronous set/reset signal, Scan Design Flow: Scan design rule checking and repair, scan synthesis, scan extraction, scan verification. Special-Purpose Scan Designs: Enhanced scan, snapshot scan, error-resilient scan, RTL Design for Testability: RTL scan design rule checking and repair, RTL scan synthesis, RTL scan extraction and scan verification. **Laboratory Sessions/ Experimental Learning:** 1. Hands-on experience in implementing scan designs, performing DFT (Design for Testability) analysis, and verifying scan functionality through simulation. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/noc/courses/noc16/SEM2/noc16-ec08/ 2. https://nptel.ac.in/courses/106103016	**8 Hrs**

UNIT-III	
Logic and Fault Simulation: Logic simulation for design verification, fault simulation for test and diagnosis, Simulation Models: Gate-level network, logic symbols, logic element evaluation, timing models, Logic Simulation: Compiled-code simulation, event-driven simulation, compiled-code *versus* event-driven simulation, hazards, Fault Simulation: Serial fault simulation, parallel fault simulation, deductive fault simulation, concurrent fault simulation, differential fault simulation, fault detection, comparison of fault simulation techniques, alternatives to fault simulation. **Laboratory Sessions/ Experimental Learning:**	**8 Hrs**

1. Understand and compare different fault simulation techniques—serial, parallel, and deductive—for assessing the testability and fault coverage of digital circuits. **Video Link / Additional Online Information:** 2. https://archive.nptel.ac.in/noc/courses/noc16/SEM2/noc16-ec08/ 3. https://nptel.ac.in/courses/106103016	
UNIT-IV	
Automatic Test Pattern Generation: Random Test Generation, Theoretical Background: Boolean Difference, Designing a Stuck-At ATPG for Combinational Circuits: A Naive ATPG Algorithm, A Basic ATPG Algorithm, Designing a Sequential ATPG: Time Frame Expansion, Gated Clocks and Multiple Clocks, Designing a Simulation-Based ATPG: Genetic-Algorithm-Based ATPG. **Laboratory Sessions/ Experimental Learning:** 1. Implement a Stuck-At Automatic Test Pattern Generation (ATPG) technique for testing stuck-at faults in combinational circuits. **Video Link / Additional Online Information:** 2. https://archive.nptel.ac.in/noc/courses/noc16/SEM2/noc16-ec08/	**8 Hrs**
UNIT-V	
Logic Built-In Self-Test: BIST design rules, test pattern generation for bist, output response analysis, BIST Architectures: BIST architectures for circuits without scan chains, BIST architectures for circuits with scan chains, BIST architectures using register reconfiguration, BIST architectures using concurrent checking circuits core-based design and test considerations, Digital Boundary Scan (IEEE Std. 1149.1): Basic concept, overall 1149.1 test architecture and operations, test access port and bus protocols, data registers and boundary-scan cells, tap controller, instruction register and instruction set, boundary-	**8 Hrs**

scan description language, on-chip test support with boundary scan, board and system-level boundary-scan control architectures, case study JTAG-based interfacing.

Laboratory Sessions/ Experimental Learning:

1. Implement Built-In Self-Test (BIST) architectures for digital circuits, focusing on both circuits without scan chains and circuits with scan chains.

Video Link / Additional Online Information:

1. https://archive.nptel.ac.in/noc/courses/noc16/SEM2/noc16-ec08/
2. https://nptel.ac.in/courses/106103016

Course Outcomes: After completing the course, the students will be able to	
CO1	Understand the principles and methodologies of design for testability (DFT) in VLSI circuits, including fault models, test pattern generation, and fault coverage metrics.
CO2	Apply DFT techniques such as scan chain insertion, built-in self-test (BIST), and boundary scan design to enhance testability of VLSI designs.
CO3	Evaluate the effectiveness of different DFT methodologies (scan design, BIST, boundary scan) in achieving high fault coverage and minimizing test complexity.
CO4	Analyze the impact of DFT strategies on chip area, power consumption, and test application time.
CO5	Assess advanced DFT techniques and their applicability to mitigate test challenges in modern VLSI designs.

Text Books:	
1.	M.Bushnell and V. D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers.
2	L.T Wang, C.W. Wu and X. Wen, “VLSI Test Principles and Architectures”, Morgan Kaufmann Publishers.
Reference Books:	

1.	T.Kropf, “Introduction to Formal Hardware Verification”, Springer Verlag, 2000
2.	L.T Wang, C.W. Wu and X. Wen, “VLSI Test Principles and Architectures”, Morgan Kaufmann Publishers. 2006.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom’s taxonomy level.

CO-PO-PSO Mapping

CO/ PO	PO1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PS0 2
CO1	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**
CO2	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**
CO3	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**
CO4	**3**	**2**	**2**	**-**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**
CO5	**3**	**2**	**2**	**2**	**-**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: V		
INTRODUCTION TO LINUX PROGRAMMING		
Course Code:	**MVJ22VL553**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40 L**	**SEE Duration: 03 Hours**

Course Learning Objectives: The students will be able to

1	Explain the fundamental concepts and architecture of the Linux operating system, including the kernel, shell, and file system.
2	Develop and compile basic C/C++ programs in the Linux environment, using standard libraries and system calls.
3	Utilize shell scripting to automate common tasks and enhance productivity in the Linux environment.
4	Apply version control systems for managing and tracking changes in Linux programming projects.
5	Assess the security implications of Linux programming practices, implementing best practices to ensure robust and secure code.

UNIT-I

Introduction to Linux: History of LINUX, architecture and features of LINUX, introduction to vi editor. **Linux commands**- PATH, man, echo, printf, script, passwd, uname, who, date, stty, pwd, cd, mkdir, rmdir, ls, cp, mv, rm, cat, more, wc, lp, od, tar, gzip, file handling utilities, security by file permissions, process utilities, disk utilities, networking commands, unlink, du, df, mount, umount, find, unmask, ulimit, ps, w, finger, arp, ftp, telnet, rlogin. **Utilities:** Text Processing utilities and backup utilities, tail, head, sort, nl, uniq, grep, egrep, fgrep, cut, paste, join, tee, pg, comm, cmp, diff, tr, awk, cpio **Laboratory Sessions/ Experimental Learning**: 1. To familiarize with basic and advanced Linux commands. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117106113	**8 Hrs**

UNIT-II	
Introduction to Shells: Linux session, standard streams, redirection, pipes, tee command, command execution, command-line editing, quotes, command substitution, job control, aliases, variables, predefined variables, options, shell/environment customization. **Filters**: Filters and pipes, concatenating files, display beginning and end of files, cut and paste, sorting, translating characters, files with duplicate lines, count characters, words or lines, comparing files. **Laboratory Sessions/ Experimental Learning:** 1. To familiarize with basic and advanced shell commands and understand the use of filters to process text data. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117106113	**8 Hrs**
UNIT-III	
Grep: Operation, grep family, searching for file content. sed: scripts, operation, addresses, commands, applications, grep and sed. UNIX file structure: Introduction to UNIX file system, inode (Index Node), file descriptors, system calls and device drivers. **File Management:** File structures, system calls for file management – create, open, close, read, write, lseek, link, symlink, unlink, stat, fstat, lstat, chmod, chown, directory api – opendir, readdir, closedir, mkdir, rmdir, umask **Laboratory Sessions/ Experimental Learning:** 1. Practice using the grep command and basic file management operations in Linux. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117106113	**8 Hrs**
UNIT-IV	
Process And Signals: Process, process identifiers, process structure: process table, viewing processes, system processes, process scheduling, starting new processes: waiting for a	**8 Hrs**

process, zombie processes, orphan process, fork, vfork, exit, wait, waitpid, exec, signals functions, unreliable signals, interrupted system calls, kill, raise, alarm, pause, abort, system, sleep functions, signal sets. **File Locking:** creating lock files, locking regions, use of read and write with locking, competing locks, other lock commands, deadlocks. **Laboratory Sessions/ Experimental Learning:** 1. Practice managing processes and signals, as well as implementing file locking mechanisms in Linux. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117106113	
UNIT-V	
Inter Process Communication: Pipe, process pipes, the pipe call, parent and child processes, and named pipes: fifos, semaphores: semget, semop, semctl, message queues: msgget, msgsnd, msgrcv, msgctl, shared memory: shmget, shmat, shmdt, shmctl, ipc status commands. **Introduction to Sockets:** Socket, socket connections - socket attributes, socket addresses, socket, connect, bind, listen, accept, socket communications. **Laboratory Sessions/ Experimental Learning:** 1. Practice inter-process communication (IPC) mechanisms using sockets in Linux. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117106113	**8 Hrs**

Course Outcomes: After completing the course, the students will be able to	
CO1	Utilize various Linux commands that are used to manipulate system operations at admin level.
CO2	Develop shell programming using Linux commands.
CO3	Design and write application to manipulate internal kernel level Linux file system.

CO4	Develop IPC-API's that can be used to control various processes for synchronization.
CO5	Develop network programming that allows applications to make efficient use of resources available on different machines in a network.
Text Books:	
1.	W. Richard. Stevens, Advanced Programming in the UNIX Environment, 3rd edition, Pearson Education, New Delhi, India.
2.	Unix and shell Programming Behrouz A. Forouzan, Richard F. Gilberg.Thomson
Reference Books:	
1.	Linux System Programming, Robert Love, O'Reilly, SPD
2.	Advanced Programming in the UNIX environment, 2nd Edition, W.R.Stevens, Pearson Education.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping													
CO/ PO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
CO1	3	3	1	2	2	-	-	-	-	-	-	2	1	1
CO2	3	3	1	2	2	-	-	-	-	-	-	2	1	1
CO3	3	3	1	2	2	-	-	-	-	-	-	2	1	1
CO4	3	3	1	2	2	-	-	-	-	-	-	2	1	1
CO5	3	3	1	2	2	-	-	-	-	-	-	2	1	1

High-3, Medium-2, Low-1

B.E. (VLSI DESIGN AND TECHNOLOGY)

Semester: V		
SIGNALS AND SYSTEM		
Course Code:	**MVJ22VL554**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40 L**	**SEE Duration: 03 Hours**

Course Learning Objectives: The students will be able to

1	Understand the mathematical description of continuous and discrete time signals and systems.
2	Analyze the signals in time domain using convolution sum.
3	Analyze the response of the LTI system to any input signal.
4	Analyze LTI systems in time and transform domains.
5	Apply the knowledge of frequency-domain representation and analysis concepts using Fourier analysis tools and Z-transform.

UNIT-I

Prerequisites: *Definition of step, ramp, impulse response.* **Introduction and Classification Of Signals**: Definition of a signal and systems, communication and control system as examples, classification of signals. **Basic Operations on Signals:** Amplitude scaling, addition, multiplication, differentiation, integration, time scaling, time shift and time reversal. **Elementary Signals/Functions**: Exponential, sinusoidal, step, impulse and ramp functions. Expression of triangular, rectangular and other waveforms in terms of elementary signals. **Laboratory Sessions/ Experimental Learning:** 1.Exploring concepts with MATLAB- Generation of both continuous time and discrete time signals of various kinds. b) Plot $y(x) = x^2\cos(x)$, $g(x) = x\cos(x)$, $f(x) = 2^x\sin(x)$, $0 \leq x \leq 2\pi$ in the same figure. 2. Generation of Signals & Signal Operations Plot in the time interval $-5 \leq t \leq 10$, the following signals: a) $\delta(t) + 2\,\delta(t)$ b) $u(t) + 2\,u(t) + 1$ c) $r(t) + u(t)$	**8 Hrs**

Applications: Time shifting operation can be used in artificial intelligence, such as in systems that use time delay neural network, multiplication of signals is exploited in the field of analog communication when performing amplitude modulation (AM), differentiation of a signal is used in the field of image or video processing. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/106/108106151/ 2. https://onlinecourses.nptel.ac.in/noc21_ee28/preview 3. https://archive.nptel.ac.in/courses/108/104/108104100/	
UNIT-II	
System Classification and Properties: Linear-nonlinear, time variant-invariant, causal-non causal, static-dynamic, stable-unstable, invertible. **Time Domain Representation of LTI System**: Impulse response of an LTI system, convolution sum, convolution integral. Properties of convolution - Commutative property, distributive property, associative property and system interconnection. Computation of convolution sum and convolution integral using graphical method for unit step and unit step, unit step and exponential, exponential and exponential, unit step and rectangular, and rectangular and rectangular. **Laboratory Sessions/ Experimental Learning:** 1.To compute convolution of two signals using MATLAB. b) A system is described by the impulse response h (t) =t, $0 \leq t \leq 10$. Compute and plot the response of the system to the input signal $x(t)=0.8^{t}$, $0 \leq t \leq 10$. c) Compute the convolution between the complex sequence =[3+2j,1+j,4+6j] and h=[1-2j,j,3-2j,2]. **Applications:** Convolution concepts are used in artificial intelligence, image processing, signal filtering, audio processing. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/106/108106151/ 2. https://archive.nptel.ac.in/courses/108/106/108106163/ 3. https://archive.nptel.ac.in/courses/108/104/108104100/	**8 Hrs**
UNIT-III	

Prerequisites: *Basics of Fourier series concepts.* **LTI System Properties in Terms of Impulse Response**: Memoryless, causal, stable, invertible, and step response. **Fourier Representation of Periodic Signals:** CTFS and DTFS definition and basic problems (excluding properties). **Laboratory Sessions/ Experimental Learning:** 1.To analyse the spectrum of signal with Fourier series using MATLAB. b) Verify the linearity property of the given periodic signals x(t)=cos(t) and y(t)=sin(2t), scalars are a=3+2j,b=2. c) Verify the time reversal property of the given periodic signal x(t)=t cos(t) ,$0 \leq t \leq 2\pi$ in one period. **Applications**: Signal processing, control theory, communications systems, image and video processing, biomedical engineering (ECG, MRI), oil extraction (Seismology), music industry (Audio) and power quality analysis. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/106/108106163/ 2. https://archive.nptel.ac.in/courses/108/104/108104100/	**8 Hrs**
UNIT-IV	
Prerequisites: *Basics of fourier transform concepts* **Fourier Representation of Aperiodic Signals**: Introduction to fourier transform, definition and basic problems. Properties of fourier transform: Linearity, time shift, frequency shift, scaling, differentiation and integration, convolution and modulation, Parseval's theorem and problems on properties of fourier transform. **Laboratory Sessions/ Experimental Learning:** 1. Application of fourier transform in modulation and demodulation technology using MATLAB. b) Compute the fourier transform of the function $x(t) = e^{-t} u(t)$ c) Suppose that a signal x(t) is given by $x(t)=te^{-3t}$. Compute the fourier transform X (w) of the signal of the signal x(t) and plot for $-20 \leq w \leq 20$ rad/sec.	**8 Hrs**

Applications: Fourier transform in modulation and demodulation technology, frequency division multiplexing and time division multiplexing, in filtering technology **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/106/108106151/ 2. https://archive.nptel.ac.in/courses/108/106/108106163/ 3. https://archive.nptel.ac.in/courses/108/104/108104100/	
UNIT-V	
Prerequisites: *Basics of Z-transform concepts.* **The Z-Transforms:** Z transform, properties of the region of convergence, properties of the Z-transform, inverse Z-transform, causality and stability, transform analysis of LTI systems. **Laboratory Sessions/ Experimental Learning:** 1.To compute Z-transform of finite duration sequence using MATLAB. b) Compute the z-transform of the sequence fx(n)-[-3,5,6,7,8], $-2 \leq n \leq 2$. c) Compute the z-transform of the discrete-time signal $x(n)= n^2 u(n)$. d) Compute the convolution between the signals $X_1(z)=$ z/z-0.9 and $X_2(z)$=z /z+6. **Applications**: In analysis of digital filters, used to simulate the continuous systems, Analyse the linear discrete system, used to finding frequency response, analysis of discrete signal, helps in system design and analysis and also checks the systems stability, for automatic controls in telecommunication. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/106/108106151/	**8 Hrs**

Course outcomes: After completing the course, the students will be able to

CO1	Explain the fundamental concepts of signals and systems, including continuous-time and discrete-time signals, linear time-invariant (LTI) systems.
CO2	Apply mathematical techniques to analyze signals in both the time and frequency domains.
CO3	Analyze the behavior of LTI systems by evaluating their impulse response, step response, and frequency response.
CO4	Implement signal processing algorithms, such as convolution and correlation, to process and interpret real-world signals.

CO5	Analyze the performance of different system representations (e.g., differential equations, difference equations, state-space models) by comparing their advantages and limitations in modeling.
Text Books:	
1.	Alan V Oppenheim, Alan S, Willsky and A Hamid Nawab, "Signals and Systems" Pearson Education Asia / PHI, 2nd edition.
2.	Simon Haykins and Barry Van Veen, "Signals and Systems", 2nd Edition, Wiley India. ISBN 9971-51-239-4.
Reference Books:	
1.	H.P Hsu, R. Ranjan, "Signals and Systems", Scham's outlines, TMH.
2.	Michael Roberts**,** "Fundamentals of Signals & Systems", 2nd edition, Tata McGraw-Hill, 2010, ISBN 978-0-07-070221-9.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have an internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

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CO-PO-PSO Mapping													
CO/ PO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
CO1	3	3	2	2	2	-	-		-	-	-	2	1	1
CO2	3	3	2	2	2	-	-	-	-	-	-	2	1	1
CO3	3	3	2	2	2	-	-	-	-	-	-	2	1	1
CO4	3	3	2	2	2	-	-	-	-	-	-	2	1	1
CO5	3	3	2	2	2	-	-	-	-	-	-	2	1	1

High-3, Medium-2, Low-1

B.E. (VLSI DESIGN AND TECHNOLOGY)

Semester: V		
INNOVATION AND ENTREPRENEURSHIP		
Course Code:	**MVJ22VL555**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40 L**	**SEE Duration: 03 Hours**

Course Learning Objectives: The students will be able to	
1	Inspired; develop entrepreneurial mindset and attributes; entrepreneurial skill sets for venture creation and intrapreneurial leadership
2	Apply the process of problem-opportunity identification and feasibility assessment by developing a macro perspective of the real market, industries, domains, and customers while using design thinking principles to refine and pivot their venture idea.
3	Analyze Customer and Market segmentation, estimate Market size, and develop and validate Customer Persona.
4	Initiate Solution design, develop MVP, and determine Product-Market fit prototypes.
5	Craft initial Business plan, Develop go-to-market strategies apply storytelling skills in presenting a persuasive and defensible Venture Pitch.

UNIT-I	
Entrepreneurship Fundamentals & Context Meaning and concept, attributes and mindset of entrepreneurial and intrapreneurial leadership, role models in each and their role in economic development. Gamified role play-based exploration aligned to one's short-term career aspiration and ambition. An understanding of how to build an entrepreneurial mindset, skillsets, attributes, and networks while on campus. **Core Teaching Tool:** Simulation, Game, Industry Case Studies (Personalized for students – 16 industries to choose from), Venture Activity	**8 Hrs**
UNIT-II	
Problem & Customer Identification: Understanding and analyzing the macro-problem and Industry perspective, technological, socio-economic, and urbanization trends and their implication on new opportunities. Identifying passion, identifying and defining problems using Design thinking principles. Analyzing problems and validating with the potential customer. Iterating problem-customer fit. Understanding customer segmentation, creating and validating customer personas. Competition and Industry trends mapping and assessing initial opportunity.	**8 Hrs**

Core Teaching Tool: Several types of activities including Class, game, Gen AI, 'Get out of the building', and Venture Activities.	
UNIT-III	
Solution design & Prototyping: Understanding Customer Jobs-to-be-done and crafting innovative solution design to map to customers' needs and create a strong value proposition. Developing Problem-solution fit iteratively. Understanding prototyping and MVP. Developing a feasibility prototype with differentiating values, features, and benefits. Initial testing for proof-of-concept and iteration on the prototype. **Core Teaching Tool:** Venture Activity, no code Innovation tools, Class activity	**8 Hrs**
UNIT-IV	
Opportunity Assessment and Sizing, Business & Financial Model: Assess relative market position via competition analysis, sizing the market, and assessing the scope and potential scale of the opportunity. Introduction to Business model and types, Lean approach, 9 block lean canvas model, riskiest assumptions to Business models. Importance of Build–Measure–Lean approach. **Business planning:** components of Business plan- Sales plan, People plan, and financial plan. Core Teaching Tool: Class and Venture Activity	**8 Hrs**
UNIT-V	
Go-to-Market Plan, Scale Outlook, and Venture Pitch Readiness: Financial Planning: Types of costs, preparing a financial plan for profitability using a financial template, understanding the basics of Unit economics, and analyzing financial performance. Introduction to Marketing and Sales, Selecting the Right Channel, creating a digital presence, and building customer acquisition strategy. Choosing a form of business organization specific to your venture, identifying sources of funds: Debt & Equity, Map the Start-up Lifecycle to Funding Options. **Scale Outlook and Venture Pitch readiness:** Understand and identify potential and aspiration for scale vis a vis your venture idea. Persuasive Storytelling and its key components. Build an Investor-ready pitch deck. **Core Teaching Tool:** Expert talks; Cases; Class activity and discussions; Venture Activities	**8 Hrs**

Course outcomes: After completing the course, the students will be able to

CO1	Understand Entrepreneurial Skillset and Mindset
CO2	Understand and analyze industry problems and Enhance customer personas based on market/other feedback

CO3	Understand and develop MVPs
CO4	Understand and apply Business models and Business planning.
CO5	Develop a go-to-market strategy and build a Persuasive sales pitch
Text Books:	
1.	Robert D. Hisrich, Michael P. Peters, Dean A. Shepherd, Sabyasachi Sinha (2020). Entrepreneurship, McGrawHill, 11th Edition
2.	Namita Thapar (2022) The Dolphin and the Shark: Stories on Entrepreneurship, Penguin Books Limited
3.	Simon Sinek (2011) Start with Why, Penguin Books Limited
Suggested Learning Sources:	
1.	Ries, E. (2011). The Lean Startup: How Today's Entrepreneurs Use Continuous Innovation to Create Radically Successful Businesses. Crown Business
2.	Osterwalder, A., & Pigneur, Y. (2010). Business Model Generation: A Handbook for Visionaries, Game Changers, and Challengers. John Wiley & Sons.
3.	Brown Tim (2019) Change by Design Revised & Updated: How Design Thinking Transforms Organizations and Inspires Innovation, Harper Business
4.	Collins Jim, Porras Jerry, (2004) Built to Last: Successful Habits of Visionary Companies
5.	Burlington Bo, (2016) Small Giants: Companies That Choose to Be Great Instead of Big
6.	Saras D. Sarasvathy, (2008) Effectuation: Elements of Entrepreneurial Expertise, Elgar Publishing Ltd

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have an internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**2**	**2**	**2**	**-**	**-**	**-**	**-**		**-**	**-**	**-**	**2**	**2**	**-**
CO2	**-**	**-**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**-**	**-**
CO3	**-**	**-**	**2**	**-**	**-**	**2**	**-**	**-**	**2**	**-**	**-**	**2**	**-**	**-**
CO4	**-**	**-**	**2**	**-**	**-**	**-**	**-**	**-**	**2**	**-**	**-**	**2**	**-**	**-**
CO5	**-**	**-**	**2**	**-**	**-**	**2**	**2**	**2**	**-**	**2**	**-**	**2**	**-**	**-**

High-3, Medium-2, Low-1

B.E (VLSI Design and Technology)

Semester: VI		
SCRIPTING LANGUAGE FOR VLSI		
Course Code:	**MVJ22VL61**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:2**	**SEE Marks: 50**
Hours:	**40L+ 26P**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Identify the purposes and features of different scripting languages, including Python, TCL/TKL, and PERL	
2	Utilize loops and conditional statements to control the flow of Python programs.	
3	Implement functions and perform basic file operations in Python.	
4	Design and develop Python scripts to automate execution, data extraction, and data manipulation tasks in VLSI design workflows	
5	Apply regular expressions (regex) for pattern matching and data extraction tasks in VLSI design files, ensuring accurate data retrieval and manipulation.	

UNIT 1	
Introduction to Scripting: Origin of scripting, different types of scripting languages python, TCL/TKL and PERL etc, objective of scripting language, **Python Basics:** Python history and features, python software environment, The python interactive shell, user input, python programming for HELLO WORLD, importance of indentation. **Python Variables and Data types:** Variables, constants, comments, strings, numbers, integer, floats, Boolean, complex. **Operators:** Arithmetic operators, assignment operators, comparison operators, logical operators, identity operators, membership operators and bitwise operators. **Project Based Learning:** 1. Enable python command line interface (CLI) interface in EDA tools and implement scripts to manage and manipulate EDA tools to create run program, checkpoints of verification and stop or exit the program through command line interface(CLI) of EDA	**8Hrs.**

tools (Xilinx-Vivado) **Laboratory Sessions/ Experimental Learning:** 1. Understand integers and floats, perform arithmetic operations. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/106/106/106106182/ **2.** https://onlinecourses.swayam2.ac.in/aic20_sp31/preview	
UNIT 2	
Conditional Loops and iterations: Conditional if-else, nested if-else, while loop, nested while, for loop, break, continue **Advanced-Data Types:** Array, list, tuple, set, and dictionaries: functions for generation, slicing, indexing, different arithmetic and logical operations etc. use of functions: grep, split, join, slice, pop, push, reverse, sort, chop. **Project Based Learning:** 1. Create a python script to run two program (verilog/VHDL) for 10 iterations and merged all generated log file into single log file **Laboratory Sessions/ Experimental Learning:** 1. Understand and use conditional statements. Implement for and while loops for iteration. **Video Link / Additional Online Information:** **1.** https://onlinecourses.swayam2.ac.in/cec22_cs20/preview **2.** https://onlinecourses.swayam2.ac.in/aic20_sp31/preview	**8Hrs.**
UNIT 3	
Functions: Introduction to using functions and modules, types of functions; parameter and argument, default argument following non-default argument, documenting functions and	**8Hrs.**

custom functions vs. standard functions turtle graphics; techniques for importing functions and modules. **Working with Files:** Files and file paths, using the / operator to join paths, working with directory, the home directory, absolute vs. relative paths, getting the parts of a file path, finding file sizes and folder contents, modifying a list of files using glob patterns, checking path validity, file reading/writing process. **Project Based Learning:** 1. Develop Python scripts to automate functions/modules for basic operations like locating log files from different sub-directories, copying, merging, moving, renaming, deletion (both permanent and safe), and compression operations. function should be generic so that targeted operation can be passed through argument, ex: for copying: python functions() arg=copy, merged **Laboratory Sessions/ Experimental Learning:** 1. Learn to define and call basic functions. **Video Link / Additional Online Information:** 1. https://onlinecourses.swayam2.ac.in/cec22_cs20/preview 2. https://onlinecourses.swayam2.ac.in/aic20_sp31/preview	
UNIT 4	
Pre-requisite: *Python os, regex library* **Organizing Files:** Copying files and folders, moving and renaming files and folders, permanently deleting files and folders, safe deletes with the send2trash module, compressing files with the zipfile module. **Regular Expression:** Finding patterns of text with regular expressions: creating regex objects, matching regex objects, review of regular expression matching, grouping with parentheses, matching multiple groups with the pipe, optional matching with the question mark, matching zero or more with the star, matching one or more with the plus, matching specific repetitions with braces, greedy and non-greedy matching.	**8Hrs.**

Project Based Learning: 1. Develop custom script function to automate common VLSI design tasks, such as file parsing, data extractions, performance parameters like hold/setup time, power, timing parameters and report generation. Targeted parameters can be passed through argument means which parameters are needed from the function.. **Laboratory Sessions/ Experimental Learning:** 1. Understand and perform basic file operations **Video Link / Additional Online Information:** 1. https://onlinecourses.swayam2.ac.in/cec22_cs20/preview 2. https://onlinecourses.swayam2.ac.in/aic20_sp31/preview	
UNIT 5	
Pre-requisite: *Python pandas NumPy library* **Working with CSV and Excel File:** Reading and writing of csv and excel file, generating csv/excel file from dictionary, merging all csv/excel file, statistical analysis (mean, media, standard deviation etc.) of data from csv file. Brief advance libraries: argv, sys, matplotlib, pyeda **Project Based Learning:** 1. Develop python scripts for post-processing of data analysis using python libraries like Pandas, Numpy, matplotlibrary, ML/DL etc. **Laboratory Sessions/ Experimental Learning:** 1. Read and write CSV files using the csv module and pandas library. **Video Link / Additional Online Information:** 1. https://onlinecourses.swayam2.ac.in/cec22_cs20/preview 2. https://onlinecourses.swayam2.ac.in/aic20_sp31/preview	**8Hrs.**

S.N.	List of Experiments
1	Print all the prime numbers between 1 and 100
2	Write a program to check whether a string or number is a palindrome or not
3	You have been given a random integer array/list(ARR) of size N. You are required to find and return the second-largest element present in the array/list. Sample input 4 3 10 9 2 and output 9. Use array or list concepts
4	Phone Number and Email Address Extractor using Python automation
5	Parsing a log File to Extract targeted “string” and store into csv file
6	Renaming Files with American-Style Dates to European-Style Dates
7	Reading, writing and update the spread sheet through python script
8	Read data from log file and keep into dictionary, then do statical analysis and post that store all data into csv file

Course Outcomes: After completing the course, the students will be able to	
CO1	Demonstrate a comprehensive understanding of the purposes, distinguishing features, and typical applications of various scripting languages such as Python, TCL/TKL, and PERL.
CO2	Utilize Python's loops (for, while) and conditional statements (if, else, elif) proficiently to control program flow in diverse scenarios.
CO3	Implement functions in Python to encapsulate reusable code segments and enhance code modularity. Integrate basic file operations within functions to manage data effectively in VLSI design and other applications.
CO4	Organize and manage files systematically using Python's file handling capabilities. Apply regular expressions (regex) to perform pattern matching and advanced text processing tasks, ensuring accurate data extraction and manipulation in VLSI design workflows.
CO5	Utilize Python libraries (such as pandas for CSV and openpyxl for Excel) to handle and analyze data stored in CSV and Excel files.

Textbooks:

1.	A. B. Downey, “Think Python, How to Think Like a Computer Scientist”, 2nd edition O′Reilly, 2015.
2	A.l.Sweigart, “Automate the boring stuff with Python: practical programming for total beginners. no starch press”, 2019.
Reference Books:	
1.	Ousterhout J. and Jones K, "Tcl and the Tk toolkit", Upper Saddle River, NJ: Addison-Wesley.
2.	Christiansen, Tom, and Nathan Torkington “Perl cookbook: Solutions & examples for Perl programmers” O'Reilly Media.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom’s taxonomy level.

CO-PO-PSO Mapping														
CO/PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**2**	**2**
CO2	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**2**	**2**
CO3	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**2**	**1**
CO4	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI Design and Technology)

Semester: VI		
ANALOG VLSI DESIGN		
Course Code: MVJ22VL62		**CIE Marks:50**
Credits: L:T:P: 3:0:2		**SEE Marks: 50**
Hours:40 L+ 26P		**SEE Duration: 03Hours**

Course Learning Objectives: The students will be able to	
1	Explain the basic physics and operational principles of MOS devices, including their structure, behavior under different bias conditions, and limitations in circuit applications.
2	Analyze the performance characteristics and applications of single-stage and differential amplifiers
3	Evaluate the principles behind current mirrors and the generation of current and voltage references, examining their stability, accuracy, and applications in analog circuit design.
4	Apply knowledge of current mirror circuits to design and implement reference current sources.
5	Design operational amplifiers (op-amps) while adhering to specified design constraints

UNIT-I	
Introduction to Analog IC Design: Motivation for analog VLSI design, and mixed signal circuits in MOS technologies and issues thereof. MOS device fundamentals: Basic MOS models, device capacitances, parasitic resistances, substrate models, transconductance, output resistance, f_T, frequency dependence of device parameters. **Laboratory Sessions/ Experimental Learning**: 1. Investigate and measure key parameters of MOSFETs, including device capacitances, parasitic resistances, substrate effects, transconductance, and output resistance. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/117/101/117101105/	**8 Hrs**
UNIT-II	

Single Stages and differential Amplifier: Single stage amplifier: basic concepts, common source stage, source follower, common-gate stage, cascode stage, choice of device models. differential amplifier: single-ended and differential operation, basic differential pair, common mode response, differential pair with MOS loads, Gilbert cell. **Laboratory Sessions/ Experimental Learning:** 1. Study the operation, gain characteristics, and common-mode rejection ratio (CMRR) of a differential pair using MOSFETs as loads. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/117/101/117101105/	**8 Hrs**

UNIT-III	
Current Mirror, Current and Voltage Reference: Basic current mirror, cascode current mirror, active current mirror and biasing techniques, low current biasing, supply insensitive biasing, temperature insensitive biasing, impact of device mismatch. **Laboratory Sessions/ Experimental Learning**: 1. Explore the operation, characteristics, and applications of active current mirrors and various biasing techniques. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/117/101/117101105/ 2. https://nptel.ac.in/courses/108106084	**8 Hrs**
UNIT-IV	
Frequency Response of Amplifiers: General considerations, miller effect, frequency responses of single stage amplifier CS amplifier, source follower, CG amplifier, cascade, differential amplifier and gain and bandwidth trade-off. feedback: Feedback topologies, effect of load, modeling input and output ports in feedback circuits.	**8 Hrs**

Laboratory Sessions/ Experimental Learning: 1. Study the frequency response characteristics of a common-source amplifier and understand its bandwidth limitations. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/117/101/117101105/	
UNIT-V	
Operational Amplifiers: Performance parameters, one-stage and two stage op amps, gain boosting, comparison, common mode feedback, input range, slew rate, power supply rejection, noise in Op Amps stability and frequency compensation: multi pole systems, phase margin, frequency compensation **Laboratory Sessions/ Experimental Learning:** 1. Study and compare the characteristics, frequency response, and gain stability of one-stage and two-stage operational amplifiers. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/117/101/117101105/	**8 Hrs**

Course Outcomes: After completing the course, the students will be able to	
CO1	Analyze and design single-stage amplifiers, including common-source, common-gate, and common-drain configurations.
CO2	Analyze and design differential amplifiers, understanding their advantages and applications in analog circuits.
CO3	Explain the principles and operation of basic and advanced current mirror circuits.
CO4	Demonstrate proficiency in designing and optimizing current mirror circuits for various applications.
CO5	Design operational amplifiers (op-amps) meeting specific design constraints such as gain, bandwidth, power consumption, and stability.
LIST OF EXPERIMENTS	
S. No.	**Experiment Name**

1.	Introduction of SPICE/ EDA tools (Cadence/Synopsys), I-V characteristics MOSFET using Cadence EDA-SPECTRE/SPICE tools and understanding of different order of open source/propriety MOS PDK model
2.	Design an singe stage common source, common gate and source follower amplifier a. Draw the schematic and verify the following i) DC, AC, and transient analysis b. Draw the layout and verify the DRC, ERC c. Layout versus schematic (LVS) verifications d. Extract RC and back annotate the same and verify the design
3.	Design a differential voltage Gain and CMRR of the differential amplifier. a. Draw the schematic and verify the following i) DC, AC, and transient analysis b. Draw the layout and verify the DRC, ERC c. Layout versus schematic (LVS) verifications d. Extract RC and back annotate the same and verify the design
4.	Design a multistage current mirror to generate reference current and also increase reference current by modulating the width (W) of reference transistor.
5.	Design a single stage amplifier as per design constraints
Text Books:	
1.	Behzad Razavi, Design of Analog CMOS Integrated Circuits", McGraw Hill Education Publication, 2017.
Reference Books:	
1.	R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation, IEEE press Wiley Fourth Edition, 2019
2.	Phillip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design" Oxford University Press Second Edition.
3.	Ken Kundert and Olaf Zinke, "The Designer's Guide to Verilog-AMS", Kluwer Academic Publishers.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

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Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

Laboratory- 50 Marks

Experiment Conduction with proper results is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

CO-PO-PSO Mapping														
CO/ PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**1**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO2	**3**	**3**	**1**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**1**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**1**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**1**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI Design and Technology)

Semester: VI		
VLSI LABORATORY-2		
Course Code:	**MVJ22VLL66**	**CIE Marks: 50**
Credits:	**L:T:P:0:0:2**	**SEE Marks: 50**
Hours:	**26P**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Demonstrate understanding of the features and capabilities of CAD tools specific to analog VLSI design.	
2	Design analog circuits using CAD tools and simulate their DC, transient, and AC characteristics.	
3	Utilize CAD tools to generate layout designs from analog circuit schematics	
4	Construct GDS (Graphic Data System) files and manage the tapeout process for fabrication of integrated circuits (ICs).	
5	Analyze and optimize complex analog designs such as operational amplifiers (OP-AMPs) and differential amplifiers using CAD tools.	

LABORATORY SESSIONS:	
PART A	
Exp. No	**Experiment Names**
1.	Introduction of SPICE/ EDA tools (Cadence/Synopsys), I-V characteristics MOSFET using Cadence EDA-SPECTRE/SPICE tools and understanding of different order of open source/propriety MOS PDK model
2.	Design a single-stage common source, common gate and source follower amplifier a. Draw the schematic and verify the following i) DC, AC, and Transient Analysis b. Draw the Layout and verify the DRC, ERC c. Layout versus Schematic (LVS) verifications d. Extract RC and back annotate the same and verify the Design
3.	Design a cascode amplifier a. Draw the schematic and verify the following

	i) DC, AC, and Transient Analysis
4.	Design of basic current sink. a. Draw the schematic and verify the following i) DC, AC, and Transient Analysis
5.	Design current sink by using negative feed-back resistor a. Draw the schematic and verify the following i) DC, AC, and Transient Analysis
PART B	
6.	Differential voltage Gain and CMRR of the differential amplifier. a. Draw the schematic and verify the following i) DC, AC, and Transient Analysis b. Layout versus Schematic (LVS) verifications c. Extract RC and back annotate the same and verify the Design
7.	Design a current mirror to generate reference current and increase reference current by modulating the width (W) of reference transistor. (Parameter will be provided during lab experiment)
8.	Design a cascode current mirror and analyse the circuits with respect to width of the transistors.
9.	Design a single stage amplifier as per design constraints like gain, f_t (Parameter will be provided during lab experiment)
10.	Design a double stage amplifier as per design constraints (Parameter will be provided during lab experiment)
Course outcomes: After completing the course, the students will be able to	
CO1	Utilize CAD tools for VLSI design, including schematic entry, simulation, layout design, and verification processes.
CO2	Design analog circuits and perform comprehensive analyses of their DC, transient, and AC characteristics.
CO3	Analyze layout designs derived from circuit schematics, performing Layout vs. Schematic (LVS) checks to verify conformity and functionality.

CO4	Construct GDS files and prepare tapeouts for integrated circuit fabrication, understanding the manufacturing process and requirements for IC production. Apply industry standards and practices to ensure compliance and readiness for fabrication.
CO5	Evaluate and optimize complex analog designs, such as operational amplifiers and differential amplifiers, analyzing performance metrics including gain, bandwidth, stability, and noise.

CO-PO-PSO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**
CO2	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**
CO3	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**
CO4	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**
CO5	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**

High-3, Medium-2, Low-1

B.E (VLSI Design and Technology)

Semester: VI		
LOW POWER VLSI DESIGN		
Course Code:	**MVJ22VL631**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40 T**	**SEE Duration: 3 Hrs**

Course Learning Objectives: The students will be able to

1	Compare and contrast the power dissipation characteristics of various digital circuit designs to identify the most significant contributors to overall power consumption.
2	Design and implement DVFS strategies in digital circuits to achieve power reduction.
3	Utilize specific design techniques to minimize switched capacitance in digital circuits.
4	Implement various leakage power reduction techniques in VLSI circuit designs.
5	Investigate and analyze the effects of different software optimization techniques on the power consumption of VLSI systems.

UNIT-1	
Introduction: Need for low power VLSI chips, sources of power dissipation in digital integrated circuits: Short circuit power dissipation, switching power dissipation**:** Dynamic power for a complex gate, reduced voltage swing, internal node power, switching activity, switching activity of static CMOS gates, inputs not equiprobable, mutually dependent inputs, transition probability in dynamic gates, power dissipation due to charge sharing, glitching power dissipation, leakage power dissipation, short channel effects **Laboratory Sessions/ Experimental Learning:** 1. Understand the basic operation of CMOS (Complementary Metal-Oxide-Semiconductor) gates. Measure and analyze the switching activity of CMOS gates. Calculate the power consumption due to switching activity. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/106/105/106105034/ 2. https://onlinecourses.nptel.ac.in/noc24_ee80/preview	**8Hrs.**
UNIT-2	

Low-Power Design Approaches: Low-power design through voltage scaling: Device feature size scaling: Constant-field scaling, constant-voltage scaling, multi-vdd circuits, voltage scaling using high-level transformations, dynamic voltage and frequency scaling: Basic approach, DVFS with varying work load, the model, workload prediction, discrete processing rate, latency overhead, adaptive voltage scaling, subthreshold logic circuits Architectural level approach–pipelining and parallel processing, multicore, and combining parallelism with pipelining **Laboratory Sessions/ Experimental Learning:** 1. Implement low-power design techniques through voltage scaling and architectural approaches, including multi-VDD circuits, dynamic voltage and frequency scaling (DVFS), and architectural-level approaches such as pipelining and parallel processing. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/106/105/106105034/ 2. https://onlinecourses.nptel.ac.in/noc24_ee80/preview	**8Hrs.**
UNIT-3	
Switched Capacitance Minimization Approaches: Introduction, system-level approach: Hardware–software codesign, Transmeta's Crusoe processor, bus encoding: Gray coding, one-hot coding, bus-inversion coding, T0 coding, clock gating: CG circuits, CG granularity, gated-clock FSMs, FSM state encoding, FSM partitioning, operand isolation, glitching power minimization, logic styles for low power: Static CMOS logic, dynamic CMOS logic. **Laboratory Sessions/ Experimental Learning:** 1. Implement FSMs using different state encoding methods. Analyze the impact of state encoding on area, speed, and power. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/106/105/106105034/ 2. https://onlinecourses.nptel.ac.in/noc24_ee80/preview	**8Hrs.**
UNIT-4	**8Hrs.**

Leakage Power Minimization Approaches: Fabrication of multiple threshold voltages, variable-threshold-voltage CMOS (VTCMOS) approach, multi-threshold-voltage CMOS (MTCMOS) approach, power gating, transistor stacking, dual-Vt assignment approach (DTCMOS), **Power Management:** Combining DVFS and power management, **Dynamic Vth Scaling** **Laboratory Sessions/ Experimental Learning:** 1. Implement the technique of using transistors with different threshold voltages (Vt) to optimize power and performance in CMOS circuits. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/106/105/106105034/ 2. https://onlinecourses.nptel.ac.in/noc24_ee80/preview	
UNIT-5	**8Hrs.**
Low-Power Software Approaches: Introduction, machine-independent software optimizations, combining loop optimizations with DVFS: Loop unrolling, loop tiling, loop permutation, strength reduction, loop fusion, loop peeling, loop unstitching, **Advanced techniques:** Brief adiabatic logic circuits, asynchronous circuits. **Laboratory Sessions/ Experimental Learning:** 1. Measure and analyze power usage of software applications. Implement and evaluate low-power software techniques. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/106/105/106105034/ 2. https://onlinecourses.nptel.ac.in/noc24_ee80/preview	

Course outcomes: After completing the course, the students will be able to	
CO1	Identify and analyze various sources of power dissipation, including dynamic, static, and short-circuit power in digital circuits.
CO2	Implement and evaluate voltage scaling and dynamic voltage and frequency scaling (DVFS) techniques to achieve power savings in digital circuits.

CO3	Apply techniques such as clock gating, operand isolation, and bus encoding to minimize switched capacitance and thereby reduce dynamic power consumption in digital designs.
CO4	Utilize various methods, including the use of high-threshold voltage transistors, sleep transistors, and body biasing to reduce leakage power in VLSI circuits.
CO5	Apply software algorithms and code to lower power usage in VLSI systems.

Text Books:	
1.	Ajit Pal, "*Low-power VLSI circuits and systems",* Springer Publication, 2015.
2.	Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley.
Reference Books:	
1.	Gary K. Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic.
2.	Jan M. Rabaey, Massoud Pedram, "Low Power Design Methodologies", Kluwer Academic.
3.	P. Chandrasekaran and R. W. Broadersen, "Low power digital CMOS design", Kluwer Academic.
4.	A Bellamour and M I Elmasri, "Low power VLSI CMOS circuit design", Kluwer Academic.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50 =100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding

up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
CO1	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**2**	**2**
CO2	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**2**	**2**
CO3	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**2**	**2**
CO4	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**2**	**2**
CO5	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**2**	**2**

High-3, Medium-2, Low-1

B.E (VLSI Design and Technology)

Semester: VI		
FPGA AND ASIC		
Course Code:	**MVJ22VL632**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40 T**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Explain the fundamental architecture, design flow, and key differences between Field-Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs).	
2	Utilize standard cell libraries and programmable logic cells in the synthesis of simple digital circuits.	
3	Assess the quality and efficiency of RTL code and schematics in terms of performance, power, and area for ASIC construction.	
4	Analyze the impact of different floor planning and placement strategies on design performance and area utilization.	
5	Implement partitioning and routing techniques to optimize a given FPGA or ASIC design.	

UNIT-1	
FPGA Basics: Introduction to FPGAs, FPGA architecture and components, FPGA design flow **ASIC Basics:** Introduction to ASICs, types of ASICs: Full-custom, semi-custom, and programmable ASICs, ASIC design flow, comparison between FPGA and ASIC, **Design Styles and Challenges:** Full-custom layout, gate-array layout, standard-cell layout, macro-cell layout and programmable logic arrays, FPGA layout and challenges in physical design **Overview of HDL language** **Laboratory Sessions/ Experimental Learning:** 1. Write and simulate basic RTL (Register-Transfer Level) designs using Verilog HDL **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc23_ee137/preview 2. https://archive.nptel.ac.in/courses/117/108/117108040/	**8Hrs.**

UNIT-2	
ASIC Library Design: Basic standard cells, library component: basic logic gates (AND, OR, NOT), complex gates, flip-flops, latches, multiplexers. Case study of any library file (.lib) for the understanding of standard library cell, different process development kit (PDK): TSMC, UMC, USMC, SCL etc. **Programmable Logic Cells or Configurable logic Block (CLB):** Xilinx : LUT: MUX and distributed SRAM, programmable interconnect, I/O block, compare with Altera and ACTEL programmable logic cells **Synthesis:** Synthesis of logic or system design in aspect of FPGA (LUT, I/O, FF etc) and ASIC (different standard cells, MUX, AND OR, NOT, Buffer etc) **Laboratory Sessions/ Experimental Learning:** 1. Design an inverter standard cell using a schematic editor. Simulate the inverter to verify its functionality. 2. Implement and test PLC designs on programmable hardware. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc23_ee137/preview 2. https://archive.nptel.ac.in/courses/117/108/117108040/	**8Hrs.**
UNIT-3	
High Level Design Entry: RTL coding using HDL, truth table representation, state diagram, flow chart, block diagram **Low-level Design Entry: Schematic entry:** Hierarchical design, the cell library, names, schematic icons & symbols, nets, schematic entry for ASICs, connections, vectored instances & buses, edit in place, attributes, netlist screener. ASIC construction: Physical design, CAD tools system partitioning, estimating ASIC size. **A Case Study:** Steps required in ASIC: RTL to GDS and FPGA: RTL to bit file **Laboratory Sessions/ Experimental Learning:** 2. Create a basic logic circuit using schematic capture. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc23_ee137/preview 2. https://archive.nptel.ac.in/courses/117/108/117108040/	**8Hrs.**

3. https://www.youtube.com/playlist?list=PLZU5hLL_713x0_AV_rVbay0pWmED799G	
UNIT-4	
Floor Planning and Placement in Aspects of FPGA and ASIC: Goals and objectives, measurement of delay in floor planning, floor planning tools, channel definition, I/O and power planning and clock planning. **Placement in Aspects of FPGA and ASIC:** Goals and objectives, min-cut placement algorithm, iterative placement improvement, time driven placement methods, physical design flow. **Laboratory Sessions/ Experimental Learning:** 1. Perform floor planning and placement for a simple FPGA design. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc23_ee137/preview 2. https://archive.nptel.ac.in/courses/117/108/117108040/	**8Hrs.**
UNIT-5	
Partitioning in ASIC and FPGA Perspective: Goals and objectives, constructive partitioning, iterative partitioning improvement, kl, fm and look ahead algorithms. **Routing in Aspects of FPGA and ASIC:** Global routing: goals and objectives, global routing methods, global routing between blocks, back- annotation. detailed routing: goals and objectives, measurement of channel density, left-edge algorithm, area-routing algorithms, multilevel routing, timing –driven detailed routing, final routing steps, special routing, circuit extraction and DRC. **Laboratory Sessions/ Experimental Learning:** 1. Perform physical partitioning for an ASIC or FPGA design **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc23_ee137/preview 2. https://archive.nptel.ac.in/courses/117/108/117108040/	**8Hrs.**

Course outcomes: After completing the course, the students will be able to	
CO1	Explain the fundamental architecture of FPGAs and ASICs, including their internal structures and functionalities.
CO2	Understand the operation and configuration of programmable logic cells (PLCs) in FPGA architectures.
CO3	Apply RTL coding techniques to describe digital circuits at the register transfer level.
CO4	Implement floor planning to define logical and physical boundaries within an ASIC or FPGA design.
CO5	Implement routing techniques to establish interconnections between partitions while minimizing delays and resource usage.

Text Books:	
1.	Michael John Sebastian Smith, "Application - Specific Integrated Circuits", Addison- Wesley Professional.
2.	Pong P Chu, "FPGA prototyping by Verilog examples: Xilinx Spartan-3 version", John Wiley & Sons, 2011.
Reference Books:	
1.	Sridhar Gangadharan, Sanjay Churiwala, "Constraining Designs for Synthesis and Timing Analysis – A Practical Guide to Synopsis Design Constraints (SDC)", Springer, 2013
2.	Naresh Maheshwari and SachinSapatnekar, "Timing Analysis and Optimization of Sequential Circuits", Springer Science and Business Media.
3.	Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations" Springer, 2011

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2

assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50 =100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PS02**
CO1	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**
CO2	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**
CO3	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**
CO4	**3**	**2**	**2**	**-**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**
CO5	**3**	**2**	**2**	**2**	**-**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI Design and Technology)

Semester: VI		
MICRO ELECTRO-MECHANICAL SYSTEMS		
Course Code:	**MVJ22VL633**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Explain the fundamental concepts of Micro-Electro-Mechanical Systems (MEMS) and their operating principles.	
2	Demonstrate the steps involved in a specific MEMS fabrication technique through a hands-on lab session.	
3	Classify MEMS sensors based on their applications and operating principles	
4	Analyze the impact of MEMS sensors on the efficiency and functionality of real-world systems.	
5	Assess the challenges and limitations of microfabrication techniques in the context of MEMS sensor development.	

UNIT-1	
Overview of MEMS and Microsystems: MEMS and microsystem, typical MEMS and microsystems products, evolution of microfabrication, microsystems and microelectronics, multidisciplinary nature of microsystems, miniaturization. applications and markets. **Laboratory Sessions/ Experimental Learning:** 1. Understanding of MEMS gas sensor in automobile industry. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/108108113	**8Hrs.**
UNIT-2	
Working Principles of Microsystems: Introduction, microsensors, microactuation, MEMS with microactuators, microaccelerometers, microfluidics. **Engineering Science for Microsystems Design:** Introduction, molecular theory of matter and inter-molecular forces, plasma physics, electrochemistry.	

Laboratory Sessions/ Experimental Learning: 2. Understanding of MEMS Accelerometer Characterization **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/108108113	**8Hrs.**
UNIT-3	
Photolithography and Deposition Techniques: Basics understanding of photolithography for pattering layer, photolithography, chemical vapor deposition (APCVD, LPCVD, PECVD), physical vapor deposition (Thermal deposition, e-beam evaporation, sputtering). **Laboratory Sessions/ Experimental Learning:** 1. Understand the basic fabrication steps of MEMS devices and test a fabricated MEMS component. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/108108113	**8Hrs.**
UNIT-4	
Overview of Micromanufacturing: Introduction, bulk micromanufacturing, surface micromachining, the LIGA process, summary on micromanufacturing**.** **Laboratory Sessions/ Experimental Learning:** 1. Details of anisotropic etching profile in Silicon wafer. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/108108113	**8Hrs.**
UNIT-5	
Understanding various MEMS sensors: Metal oxide semiconductor gas sensor, pressure sensors, proximity sensors, gyroscope, TPMS, temperature sensor **Laboratory Sessions/ Experimental Learning:** 1. Calibrate and test a MEMS pressure sensor and evaluate its performance characteristics, such as linearity, sensitivity, and hysteresis. **Video Link / Additional Online Information:**	**8Hrs.**

1.https://nptel.ac.in/courses/108108113	

Course outcomes: After completing the course, the students will be able to	
CO1	Compare different MEMS technologies in terms of their functionality, applications, and limitations.
CO2	Apply these design and fabrication processes to create simple MEMS structures in a laboratory setting.
CO3	Use mathematical tools to model the behavior and performance of MEMS devices.
CO4	Illustrate specific applications of MEMS devices through real-world examples and case studies.
CO5	Demonstrate the micromanufacturing techniques by designing and fabricating simple microstructures.

Text Books:	
1.	Tai-Ran Hsu: "MEMS & Microsystems Design Manufacture and nanoscale Engineering", 2nd Edition, Tata McGraw Hill.
Reference Books:	
1.	Microsystem Design, Kluwer Academic Publisher, J.D. Plummer, M.D. Deal, P.G. Griffin
2.	Silicon VLSI Technology, Pearson Education, S.M. Sze (Ed)

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50 =100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PS02**
CO1	**3**	**2**	**2**	**2**	**1**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**
CO2	**3**	**2**	**2**	**2**	**1**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**
CO3	**3**	**2**	**2**	**2**	**1**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**
CO4	**3**	**2**	**2**	**2**	**1**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**
CO5	**3**	**2**	**2**	**2**	**1**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**

High-3, Medium-2, Low-1

B.E. (VLSI Design and Technology)

Semester: VI		
SOC DESIGN		
Course Code:	**MVJ22VL634**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Explain the core features, instruction sets, and pipeline structure of ARM processors.	
2	Compare the ARM architecture with other processor architectures in terms of performance, efficiency, and design complexity.	
3	Implement and optimize a digital system using ARM cores with a focus on performance, power efficiency, and real-time capabilities.	
4	Assess the benefits and limitations of advanced ARM features and extensions in various application scenarios.	
5	Analyze specific case studies to identify how ARM-based SoCs address application-specific requirements and challenges.	

UNIT 1	
ARM Organization and Implementation: 3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution, ARM implementation, The ARM coprocessor interface. **The ARM Instruction Set:** Introduction, exceptions, conditional execution, branch and branch with link (B, BL), and eXchange (BX, BLX), software interrupt (SWI), data processing instructions, multiply instructions, count leading zeros (CLZ - architecture v5T only), single word and unsigned byte data transfer instruction, half-word and signed byte data transfer instructions, multiple register transfer instructions, swap memory and register instructions (SWP), program status register instructions, coprocessor instructions, coprocessor data operations, coprocessor data transfers, coprocessor register transfers, breakpoint instruction (BRK - architecture v5T only), unused instruction space, memory faults, ARM architecture variants. **Laboratory Sessions/ Experimental Learning:**	**8Hrs.**

1. Implement and analyze the performance of a 3-stage and a 5-stage pipeline. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc24_ee17/preview	
UNIT 2	
Architectural Support for High-Level Languages: abstraction in software design, data types, floating-point data types, the ARM floating-point architecture, expressions, conditional statements, loops, functions and procedures, use of memory, run-time environment. **Architectural Support for System Development:** The ARM memory interface, the advanced microcontroller bus architecture (AMBA), The ARM reference peripheral specification, hardware system prototyping tools, the ARMulator, The JTAG boundary scan test architecture, The ARM debug architecture, embedded trace, signal processing support. **Laboratory Sessions/ Experimental Learning:** 1. Understand the floating-point unit (FPU) in ARM Cortex-M4 or similar processors by implementing and analyzing floating-point operations. At last, compare the performance of floating-point operations with integer operations. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc24_ee17/preview	**8Hrs.**
UNIT 3	
ARM Processor Cores: ARM7TDMI, ARM8, ARM9TDMI, ARM10TDMI, discussion, example and exercises. **Memory Hierarchy:** Memory size and speed, on-chip memory, caches, cache design - an example, memory management, examples and exercises	**8Hrs.**

Laboratory Sessions/ Experimental Learning: 1. Understand the architecture and functioning of ARM processor cores and compare the performance of different ARM cores **Video Link / Additional Online Information:** 1 https://onlinecourses.nptel.ac.in/noc24_ee17/preview	
UNIT 4	
Architectural Support for Operating Systems: An introduction to operating systems, The ARM system control coprocessor, CP15 protection unit registers, ARM protection unit, CP15 MMU registers, ARM MMU architecture, synchronization, context switching, input/ output, example and exercises. **Laboratory Sessions/ Experimental Learning:** 1. Understand the functionality of the memory management unit (MMU) in ARM processors. Configure and use the MMU to manage memory in an ARM-based system. Analyze the performance impact and behavior of the MMU in terms of memory access and virtual memory management. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc24_ee17/preview	**8Hrs.**
UNIT 5	
ARM CPU Cores: The ARM710T, ARM720T and ARM740T, The ARM810, The strong ARM SA-110, The ARM920T and ARM940T, The ARM946E-S and ARM966E-S, the ARM1020E, discussion, example and exercises. **Embedded ARM Applications:** The VLSI Ruby II advanced communication processor, The VLSI ISDN subscriber processor, The One C™VWS22100 GSM chip, The Ericsson-VLSI bluetooth baseband controller, examples and exercises.	**8Hrs.**

Laboratory Sessions/ Experimental Learning: 1. Understand the architecture and functionality of the Ericsson-VLSI Bluetooth Baseband Controller. Configure and use the Bluetooth Baseband Controller to establish a Bluetooth connection. Analyze the data transfer and performance of the Bluetooth connection. **Video Link / Additional Online Information:** https://onlinecourses.nptel.ac.in/noc24_ee17/preview	

Course Outcomes: After completing the course, the students will be able to	
CO1	Apply the 3- and 5-stage pipeline ARM processor cores and analyse the implementation issues.
CO2	Make use of concepts and methodologies employed in designing a System- on-chip (SoC) based around a microprocessor core and in designing the microprocessor core itself.
CO3	Understand how SoCs and microprocessors are designed and used, and why a modern processor is designed the way that it is.
CO4	Utilize integrated ARM CPU cores (including Strong ARM) that incorporate full support for memory management.
CO5	Analyze the requirements of a modern operating system and use the ARM architecture to address the same.

Text Books:	
1.	Steve Furber, ARM System-on-Chip Architecture, Second Edition, Pearson, 2015.
Reference Books:	
1.	Joseph Yiu, The Definitive Guide to the ARM Cortex-M3, Newnes, (Elsevier), 2nd Edition.
2.	Sudeep Pasricha and NikilDutt, On-Chip Communication Architectures: System on Chip Interconnect, Morgan Kaufmann Publishers.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO10**	**PO11**	**PO12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**

High-3, Medium-2, Low-1

B.E. (VLSI Design and Technology)

Semester: VI		
SEMICONDUCTOR DEVICES		
Course Code:	**MVJ22VL641**	**CIE Marks: 50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Compare the electrical properties of intrinsic and extrinsic semiconductors based on their carrier concentration and doping levels.	
2	Solve problems related to electrical conduction in semiconductors, incorporating concepts like mobility, drift velocity, and diffusion coefficient.	
3	Illustrate the I-V characteristics of a PN junction through practical experiments or simulations.	
4	Assess the impact of various physical parameters on the performance and characteristics of MOS devices.	
5	Analyze the challenges and limitations associated with scaling semiconductor devices and propose potential solutions.	

UNIT 1	
Semiconductor Fundamentals: Charge carriers in solids, fermi level, carrier concentration in semiconductors, intrinsic and extrinsic semiconductors, equilibrium concentration, Boltzmann statistics, and direct and indirect band-gap. **Carrier Transport in Semiconductors:** Current flow mechanisms: drift current, diffusion current, mobility of carriers, current density equations. **Laboratory Sessions/ Experimental Learning:** 1. Measure the sheet resistance of Silicon wafer **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/108/108108122/	**8Hrs.**
UNIT 2	

P-N Junction: Poisson equation, electric fields and potentials, p-n junction under applied bias, static current-voltage characteristics of p-n junctions, breakdown mechanisms. **Laboratory Sessions/ Experimental Learning:** 1. Study the I-V characteristics of a PN junction diode **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/108/108108122/	**8Hrs.**
UNIT 3	
MOS Capacitor: Ideal MOS fundamentals**,** accumulation, depletion and inversion, threshold voltage, oxide and interface charges, CV characteristics of MOS **Laboratory Sessions/ Experimental Learning:** 1. Measure C-V of n channel MOSFET **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/108/108108122/	**8Hrs.**
UNIT 4	
MOSFETs: Theory of operation, I_D-V_D characteristics, I_D-V_G characteristics, scaling and short channel effects, breakdown. **Laboratory Sessions/ Experimental Learning:** 1. Examine the I-V characteristics of an n-channel MOSFET. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/108/108108122/	**8Hrs.**
UNIT 5	
Optoelectronic devices: III-V semiconductors, optical absorption, direct and indirect band-gaps, solar cells, light emitting diode (LED), LASER diode **Laboratory Sessions/ Experimental Learning:**	**8Hrs.**

1. Analyze the I-V characteristics of a solar cell and determine its efficiency and fill factor. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/108/108108122/	

Text Books:	
1.	Advanced semiconductor fundamentals Book by Robert F. Pierret
2.	SEMICONDUCTOR DEVICE FUNDAMENTALS Book by Robert F. Pierret

Reference Books:	
1.	Streetman, B. and Banerjee, S., Solid State Electronics, Prentice Hall India.
2.	Sze, S.M., Physics of Semiconductor Devices, John Wiley.
Course Outcomes: After completing the course, the students will be able to	
CO1	Compare the electronic properties of semiconductors with different doping levels and analyze their band structures.
CO2	Evaluate the performance of PN junction diodes under various biasing conditions and explain the underlying physical mechanisms.
CO3	Analyze the impact of different materials and fabrication processes on the performance of MOSCAPs.
CO4	Assess the performance of MOSFETs by analyzing their characteristics in different regimes and explain the influence of physical parameters on their operation.
CO5	Compare the performance of III-V semiconductor devices with silicon-based devices and analyze their advantages and limitations in specific applications.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping													
CO/PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**2**	**2**
CO2	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**2**	**2**
CO3	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**2**	**2**
CO4	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI Design and Technology)

Semester: VI		
DIGITAL LOGIC DESIGN		
Course Code:	**MVJ22VL642**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40 L**	**SEE Duration: 03 Hours**

Course Learning Objectives: The students will be able to	
1	Design combinational digital circuits using logic gates based on simplified Boolean expressions.
2	Compare the performance and complexity of synchronous and asynchronous sequential circuits in various applications.
3	Design and implement combinational and sequential circuits for specific applications.
4	Design sequential circuits using SR, JK, D, and T flip-flops and implement state machines.
5	Use programmable devices to implement and test digital circuits.

UNIT-I	
Principles of Combinational Logic: Number systems, Boolean algebra, logic gates, canonical forms, generation of switching equations from truth tables, Karnaugh maps-3, 4 variables, incompletely specified functions (Don't care terms). **Laboratory Sessions/ Experimental Learning:** 1. Study of Logic Gates – NOT, OR, AND, NOR, NAND, XOR and XNOR. 2. Design a 4-bit Binary to Gray code converter using logic gates. **Applications:** OR gate in detecting exceed of threshold values and producing command signal for the system and AND gate in frequency measurement. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/105/108105132/	**8 Hrs**

UNIT-II	
Design and Analysis of Combinational Logic: Full adder & subtractors, parallel adder and subtractor, look ahead carry adder, binary comparators, decoder, encoders, multiplexers & demultiplexer.	**8 Hrs**

Laboratory Sessions/ Experimental Learning: 1. Design a full adder with two half adders using logic gates. 2. Design an adder cum subtractor circuit which adds when input bit operation=1 or subtract if 0, using logic gates. **Applications:** Communication systems, Speed synchronization of multiple motors in industries. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/105/108105132/	
UNIT-III	
Flip-Flops and its Applications: Latches and flip flops, master-slave jk flip-flop, timing concerns in sequential circuits, shift registers – SISO, SIPO, PISO, PIPO, universal shift register, counters – synchronous and asynchronous. **Laboratory Sessions/ Experimental Learning:** 1. Develop SR, D, JK &T flip flop using logic gates 2. Design a 6-bit Register using D-Flipflop **Applications:** Frequency divider circuit, frequency counter. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/105/108105132/	**8 Hrs**
UNIT-IV	
Sequential Circuit Design: Characteristic equations, design of a synchronous mod-n counter using clocked JK, D, T and SR flip-flops. **Laboratory Sessions/ Experimental Learning:** 1. Design a Synchronous Counter for a given sequence- 0, 2, 4, 6, 0 **Applications:**Data synchronizer, Counter. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/105/108105132/	**8 Hrs**
UNIT-V	
Applications of Digital Circuits: Design of a sequence detector, guidelines for construction of state graphs, design example – code converter.	**8 Hrs**

Programmable Logic Devices: PLA, PAL, FPGA. **Laboratory Sessions/ Experimental Learning:** 1. Designing of sequence detector using necessary digital components. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117108040/	

Course outcomes:	
CO1	Apply K-maps and Quine-McCluskey technique to simplify Boolean expressions with multiple variables.
CO2	Design combinational logic circuits based on given specifications and simplified Boolean functions.
CO3	Develop and implement combinational and sequential circuits for practical applications, considering timing, area, and power constraints.
CO4	Design sequential circuits using various flip-flops and state machine models to achieve desired sequential logic operations.
CO5	Utilize programmable devices to implement and prototype digital circuits, demonstrating flexibility and reconfigurability.

Text Books:	
1.	Morris Mano, ―Digital Design, Prentice Hall of India, Third Edition.
2.	Donald D. Givone, "Digital Principles and Design", McGraw Hill.

Reference Books:	
1.	John M Yarbrough, "Digital Logic Applications and Design", Thomson Learning.

CO-PO-PSO Mapping														
CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
CO1	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**3**	**-**	**-**	2	**1**	**1**
CO2	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**3**	**-**	**-**	**2**	**1**	**1**
CO3	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**3**	**-**	**-**	**2**	**1**	**1**
CO4	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**3**	**-**	**-**	**2**	**1**	**1**
CO5	**3**	**3**	**3**	**3**	**2**	**1**	**-**	**-**	**3**	**-**	**-**	**2**	**1**	**1**

High-3, Medium-2, Low-1

B.E. (VLSI Design and Technology)

Semester: VI		
FUNDAMENTALS OF MICROPROCESSOR AND MICROCONTROLLER		
Course Code:	**MVJ22VL643**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Explain the architecture of ARM microcontrollers, including core components such as CPU, memory, buses, and peripherals.	
2	Draw block diagrams and explain the functional units of the 8086 microprocessor architecture.	
3	Evaluate the efficiency of different interfacing techniques used to connect the 8086 microprocessor with memory, I/O devices, and external peripherals.	
4	Identify various types of peripheral devices that can be interfaced with ARM microcontrollers	
5	Design and implement embedded systems projects that integrate both microprocessors and microcontrollers to meet specific application requirements.	

UNIT 1	
The x86 microprocessor: Brief history of the x86 family, inside the 8088/86, introduction to assembly programming, introduction to program segments, the stack, flag register, x86 addressing modes. assembly language programming: directives & a sample program, assemble, link & run a program, more sample programs, control transfer instructions, data types and data definition, full segment definition, flowcharts and pseudo code **Laboratory Sessions/ Experimental Learning:** 1. Understand the basic instruction set of the 8086 microprocessor by writing and executing a simple program that adds two numbers. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117104072	**8Hrs.**

UNIT 2	
x86: Instructions sets description, arithmetic and logic instructions and programs: unsigned addition and subtraction, unsigned multiplication and division, logic instructions, rotate instructions. **INT 21H and INT 10H Programming:** Bios INT 10H programming, DOS interrupt 21H. 8088/86 interrupts, x86 PC and interrupt assignment. **Laboratory Sessions/ Experimental Learning:** 1. Explore the 8086 instruction set by writing and executing a program that demonstrates data transfer and arithmetic operations. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117104072	**8Hrs.**
UNIT 3	
Signed Numbers and Strings: Signed number arithmetic operations, string operations. memory and memory interfacing: memory address decoding, data integrity in RAM and ROM, 16-bit memory interfacing. **8255 I/O programming:** I/O addresses MAP ofx86 PC's, programming and interfacing the 8255 **Laboratory Sessions/ Experimental Learning:** 1. Demonstrate the programming of the 8255 programmable peripheral interface (PPI) to control LEDs connected to its ports using the 8086 microprocessor. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117104072	**8Hrs.**
UNIT 4	
ARM Embedded Systems: The RISC design philosophy, The ARM design philosophy, embedded system hardware, embedded system software **ARM Processor Fundamentals:** Registers, current program status register, pipeline,	**8Hrs.**

exceptions, interrupts, and the vector table, core extensions **Laboratory Sessions/ Experimental Learning:** 1. Execute simple assembly programs on an ARM-based system or emulator. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117104072	
UNIT 5	
Introduction to the ARM Instruction Set: Data processing instructions, branch instructions, software interrupt instructions, program status register instructions, coprocessor instructions, loading constants **Laboratory Sessions/ Experimental Learning:** 1. Execute assembly programs that demonstrate various instructions and their functionalities. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117104072	**8Hrs.**

Course Outcomes: After completing the course, the students will be able to

CO1	Compare the advantages and limitations of using microprocessors versus microcontrollers in different real-world scenarios.
CO2	Develop software applications using ARM microcontrollers to perform tasks such as data processing, control, and communication.
CO3	Utilize ARM architecture features to optimize code execution and memory management in embedded applications.
CO4	Implement interfacing techniques to connect peripherals such as sensors, actuators, and communication modules to x86 and ARM-based systems.
CO5	Develop and implement interrupt service routines (ISRs) to manage and respond to external events from interfaced devices.

Text Books:	
1.	Andrew N Sloss, Dominic Symes and Chris Wright, ARM system developers guide, Elsevier, Morgan Kaufman publishers, 2008.
2.	Muhammad Ali Mazidi, Janice Gillispie Mazidi, Danny Causey, The x86 PC Assembly Language Design and Interfacing, 5th Edition, Pearson, 2013.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO 1	PSO 2
CO1	3	3	2	2	1	1	1	-	1	-	-	1	1	1
CO2	3	3	2	2	1	1	1	-	1	-	-	1	1	1
CO3	3	3	2	2	1	1	1	-	1	-	-	1	1	1
CO4	3	3	2	2	1	1	1	-	1	-	-	1	1	1
CO5	3	3	2	2	1	1	1	-	1	-	-	1	1	1

High-3, Medium-2, Low-1

B.E. (VLSI Design and Technology)

Semester: VI		
FLEXIBLE ELECTRONICS		
Course Code:	**MVJ22VL644**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**

Course Learning Objectives: The students will be able to

1	Explain the significance of large area and flexible electronics in modern technology, highlighting advantages such as portability, durability, and versatility.
2	Apply knowledge to select appropriate manufacturing processes and equipment based on specific requirements for flexible electronics production.
3	Analyze the interactions and interfaces between materials and substrates in large area and flexible electronic devices to optimize performance and reliability.
4	Identify the criteria for selecting materials for flexible electronics, including mechanical flexibility, thermal stability, and compatibility with manufacturing processes.
5	Develop process flow diagrams and protocols for manufacturing large area and flexible electronic devices tailored to specific application requirements.

UNIT 1	
Introduction to Flexible Electronics and their Materials Systems: Background and history, trends, emerging technologies, general applications. **Introduction to Semiconductors and Processing Methods for Flexible Devices:** Carrier transport, doping, band structure, thin-film electronic devices. thin-film deposition and processing methods for flexible devices -CVD, PECVD, PVD, etching, photolithography, low-temperature process integration **Laboratory Sessions/ Experimental Learning:** 1. Familiarization with the fundamental processing techniques used in the fabrication of flexible electronic devices **Video Link / Additional Online Information:** 1. https://youtu.be/tRel4WbQNdU	**8Hrs.**
UNIT 2	
Materials for Flexible and Printed Electronics: Nanowire and nanoparticle synthesis, transition metal oxides, amorphous thin films, polymeric semiconductors, structure and	**8Hrs.**

property relationships, paper-based electronics, textile substrates, barrier materials. **Laboratory Sessions/ Experimental Learning:** 1. Understanding the various materials used in flexible and printed electronics, their properties, and how they are processed **Video Link / Additional Online Information:** 1. https://youtu.be/P3BSQgLfLTY	
UNIT 3	
Thin Film Transistors: Device structure and performance: I-V characteristics, gradual channel approximation, electrical stability, lifetime extraction, characterization methods for rigid and flexible devices. Metal oxide TFT's, carbon nanotube TFT's **Laboratory Sessions/ Experimental Learning:** 1. Understand the structure of thin film transistors (TFTs) and to characterize their electrical properties. **Video Link / Additional Online Information:** 1. https://youtu.be/P3BSQgLfLTY	**8Hrs.**
UNIT 4	
Solution-based Patterning Processes: Ink-jet printing, gravure, imprint lithography, spray pyrolysis, surface energy effects, multilayer patterning, design rule considerations. substrates for flexible electronics **Laboratory Sessions/ Experimental Learning:** 1. Explore solution-based patterning techniques for fabricating flexible electronic devices. Learn about various materials, deposition methods, and patterning techniques used in solution-based processing**.** **Video Link / Additional Online Information:** 1. https://youtu.be/4LiWoZDQ3E4	**8Hrs.**
UNIT 5	
Organic and Inorganic Electronic Devices: Contacts and interfaces to organic and inorganic electronic devices, schottky contacts, defects, carrier recombination, effect of applied mechanical strain., applications	**8Hrs.**

Laboratory Sessions/ Experimental Learning: 1. Investigate the electrical properties of contacts and interfaces in organic and inorganic electronic devices. **Video Link / Additional Online Information:** 1. https://youtu.be/7in7KAZgvgQ	

Course Outcomes: After completing the course, the students will be able to	
CO1	Apply material selection criteria to choose appropriate materials for different components of flexible electronic devices, such as substrates, conductive materials, and encapsulation layers.
CO2	Implement fabrication processes to construct prototype flexible electronic devices, demonstrating knowledge of material handling and process optimization.
CO3	Select appropriate fabrication techniques based on specific application requirements for flexible electronics, considering factors like resolution, throughput, and material compatibility.
CO4	Design thin film devices and circuits for specific flexible electronics applications, considering performance parameters like mobility, on/off ratio, and power consumption.
CO5	Demonstrate proficiency in using modeling to analyze the behavior and performance of materials and devices in flexible electronics applications.

Text Books:	
1.	Flexible Electronics – Materials and applications, William S Wong, Salleo, Alberto, 2009, Springer, ISBN 978-0-387-74363-9
2.	Large Area and Flexible Electronics, Mario Carioni, Yong-Yong Noh, 2015, Wiley ISBN: 978- 3-527-67999-7

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	2	2	1	-	-	-	-	-	-	1	2	2
CO2	3	3	2	2	1	-	-	-	-	-	-	1	2	2
CO3	3	3	2	2	1	-	-	-	-	-	-	1	2	2
CO4	3	3	2	2	1	-	-	-	-	-	-	1	1	1
CO5	3	3	2	2	1	-	-	-	-	-	-	1	1	1

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: VII		
SYSTEM VERILOG FOR VERIFICATION		
Course Code:	**MVJ22VL71**	**CIE Marks: 50**
Credits:	**L:T:P: 3:0:2**	**SEE Marks: 50**
Hours:	**40L+26P**	**SEE Duration: 3 Hrs.**

Course Learning Objectives: The students will be able to	
1	Explain the fundamental syntax and features of SystemVerilog, including data types, operators, and control flow constructs, specifically in the context of verification.
2	Develop SystemVerilog testbenches to verify the functionality of digital designs, utilizing constructs such as assertions, randomization, and functional coverage.
3	Apply debugging techniques using SystemVerilog to identify and resolve issues in digital design verification, utilizing tools such as simulators and waveform viewers.
4	Utilize threads and inter-process communication in test benches.
5	Evaluate the coverage and completeness of SystemVerilog verification environments, using coverage metrics and reports to assess the thoroughness of the verification process.

UNIT-I	
Verification Guidelines: The verification process, basic test bench functionality, directed testing, methodology basics, constrained random stimulus, randomization, functional coverage, test bench components, layered testbench, testbench performance **Data Types:** Built in data types, fixed and dynamic arrays, queues, associative arrays, linked lists, array methods, choosing a storage type, creating new types with typedef, creating user defined structures, typeconversion, enumerated types, constants and strings, expression width. **Laboratory Sessions/ Experimental Learning:** 1. Write a simple module that uses logic and wire to model a basic combinational circuit. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/108/108108122/	**8 Hrs**
UNIT-II	

Procedural Statements and Routines: Procedural statements, tasks, functions and void functions, task and function overview, routine arguments, returning from a routine, local data storage, time values. **Converting the Test Bench and Design:** Separating the test bench and design, the interface construct, stimulus timing, interface driving and sampling, system verilog assertions. **Laboratory sessions/ Experimental Learning:** 1. Write a SystemVerilog module with immediate assertions to check for specific conditions (e.g., reset signal activation). **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/108/108108122/	**8 Hrs**
UNIT-III	
Basic OOP and Randomization: Basic OOP: Introduction, think of nouns. not verbs, your first class, where to define a class, OOP terminology, creating new objects, object deallocation, using objects, static variables vs. global variables, class methods, detining methods outside of the class, scoping rules, using one class inside another, understanding dynamic objects, copying objects, public vs. local **Randomization:** Introduction, randomization in system verilog, constraint details, solution probabilities, valid constraints, inline constraints, random number functions, common randomization problems, iterative and array constraints, random control, random number generators. **Laboratory Sessions/ Experimental Learning**: 1. Write a SystemVerilog module that generates random values for a simple signal (e.g., a 4-bit bus). **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/108/108108122/	**8 Hrs**
UNIT-IV	
Threads and Interprocess Communication: Working with threads, disabling threads, interprocess communication, events, semaphores, mailboxes, building a test bench with threads and interprocess communication. **Laboratory Sessions/ Experimental Learning:**	**8 Hrs**

1. Write a SystemVerilog module that creates two parallel threads using fork and join to perform independent tasks (e.g., toggling two different signals). **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/108/108108122/	
UNIT-V	
Functional Coverage: Coverage types, coverage strategies, simple coverage example, anatomy of cover group and triggering a cover group, data sampling, cross coverage, generic cover groups, coverage options, analyzing coverage data, measuring coverage statistics during simulation. **Laboratory Sessions/ Experimental Learning:** 1. Write a SystemVerilog covergroup for a simple DUT, such as an ALU, to cover different operation modes (addition, subtraction, etc.). **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/108/108108122/	**8 Hrs**

Course Outcomes: After completing the course, the students will be able to	
CO1	Demonstrate proficiency in using procedural statements, tasks, functions, and interface constructs in SystemVerilog.
CO2	Implement object-oriented programming principles and constrained randomization techniques in System Verilog.
CO3	Utilize threads and inter-process communication mechanisms in System Verilog testbenches
CO4	Analyze and measure functional coverage in simulations, utilizing functional coverage metrics
CO5	Evaluate the effectiveness of different SystemVerilog verification strategies, identifying and optimizing areas for improvement to ensure comprehensive design validation.
LIST OF EXPERIMENTS	
S. No.	**Experiment Name**
1.	Write test benches for basic gates and FFs
2.	Write a testbench using TASK and FUNCTION for half adder and full adder

3.	Write a testbench for multiplier using randomization concepts.
4.	Write a testbench using OOP concepts of system verilog to verify the functionality of simple ALU of functions ADD, SUB, OR, AND and SHIFT etc. Model should not be used in practice as it fails when v > surface potentials.
5.	Write a testbench to verify ALU using functional coverage concepts of system verilog.
6.	write a testbench to verify 4 bit counter using functional coverage and randomization concepts of system verilog.
7.	write a testbench to verify a simple comparator using system assertion
8.	Write a testbench to verify 4 bit counter using threads and interprocess communication system verilog.

Text Books:	
1.	Spear, Chris. SystemVerilog for Verification: A Guide to Learning the Testbench Language Features. Springer Science & Business Media.
Reference Books:	
1.	Ashok B Mehta, "System Verilog Assertions and Functional Coverage" Springer International Publishing, 2020.
2.	Stuart Sutherland, Simon Davidmann, and Peter Flake, "System Verilog for design: A guide to using system verilog for hardware design" Springer

CO-PO-PSO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**2**	**2**
CO2	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**2**	**2**
CO3	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**2**	**2**
CO4	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**1**

High-3, Medium-2, Low-1

B.E (VLSI DESIGN AND TECHNOLOGY)

Semester: VII		
MIXED SIGNAL VLSI DESIGN		
Course Code:	**MVJ22VL72**	**CIE Marks: 50**
Credits:	**L: T:P: 3:0:2**	**SEE Marks: 50**
Hours:	**40L+26P**	**SEE Duration: 3 Hrs.**

Course Learning Objectives: The students will be able to	
1	Explain the fundamental concepts and techniques of mixed-signal VLSI design, including the principles of analog and digital circuit integration.
2	Describe the key components and architectures used in mixed-signal systems, such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and phase-locked loops (PLLs).
3	Model mixed-signal behavior using Verilog-AMS.
4	Analyze the performance characteristics of DAC circuits to evaluate and optimize their performance.
5	Analyze various ADC architectures.

UNIT-I	
Pre-requisite: *Analog VLSI design* **Introduction:** An overview, analog and mixed-signal integrated design concepts, **Revision of Analog VLSI design:** MOSFET, single stage, differential and Op-Amp Amplifier. **Advanced Analog Circuits:** Basic switched capacitor, active integrator, sample-and-hold amplifier. **Laboratory Sessions/ Experimental Learning:** 1. Design and simulate a differential amplifier using an electronic design automation (EDA) tool. Analyze the DC operating point, small-signal parameters, and frequency response of the differential amplifier. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/108/108108122/	**8 Hrs**
UNIT-II	

Verilog A/AMS for Modeling: Hardware description languages, the verilog family of languages, mixed-signal simulators, applications of verilog-ams, traditional approaches to mixed-signal design, **Mixed-Signal Modeling:** Modeling discrete behavior, modeling mixed-signal behavior, structural Verilog-AMS. **Verilog A Language for AMS Modeling: Basics:** Comments, identifiers, keywords, compiler directives, **Data Types:** Constants, variables, parameters, natures and disciplines, ports, nets, and nodes, branches **Laboratory sessions/ Experimental learning:** 1. Design a mixed-signal system using structural Verilog-AMS, such as a digital control logic driving an analog filter. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/108/108108122	**8 Hrs**
UNIT-III	
Verilog A Language for AMS Modeling: Signals: Continuous-time signal access, contributions, expressions: operators, functions, mathematical functions, logical functions, environment functions, analog operators, thresholding functions, limiting functions, small-signal stimulus functions, user-defined functions. System functions and tasks, analog behaviour, discrete-event behaviour, mixed behaviour and design hierarchy. **Laboratory Sessions/ Experimental Learning:** 1. Write a Verilog-A module to model a simple RC circuit and analyze the continuous-time response. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/108/108108122/	**8 Hrs**
UNIT-IV	
Data Converter Fundamental: Analog versus discrete time signals, converting analog signals to digital signals, sample-and-hold (S/H) characteristics, digital-to-analog converter (DAC) specifications, analog-to-digital converter (ADC) specifications, mixed-signal layout issues. **Data Converter Architectures: DAC Architectures:** Digital input code, resistor string, current steering, DAC trimming or calibration, glitch	**8 Hrs**

Laboratory Sessions/ Experimental Learning: 1. Design and simulate various DAC architectures using electronic design automation (EDA) tools. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/108/108108122/	
UNIT-V	
Data Converter Architectures: ADC Architecture: Slope ADC, SAR ADC, flash ADC, pipelined ADC and delta sigma ADC **Laboratory Sessions/ Experimental Learning:** 1. Design and simulate various ADC architectures using electronic design automation (EDA) tools. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/108/108/108108122/	**8 Hrs**

Course Outcomes: After completing the course, the students will be able to	
CO1	Demonstrate a thorough understanding of the fundamental concepts and principles of analog VLSI design
CO2	Apply Verilog-AMS to model and simulate the behavior of mixed-signal systems, integrating both analog and digital components to accurately represent real-world circuits and systems.
CO3	Utilize Verilog-A for the modeling and simulation of analog behavior
CO4	Understand the operating principles, design considerations, and performance characteristics of digital-to-analog converters (DACs) and analog-to-digital converters (ADCs).
CO5	Analyze and compare various ADC architectures, understanding their design trade-offs, applications, and performance implications in different signal processing contexts.

LIST OF EXPERIMENTS

S. No.	**Experiment Name**
1.	Write a Verilog-A model for linear conductor/resistor, capacitor and Inductor.
2.	Write a Verilog-A/MS models for a linear shunt RLC.

3.	Write a Verilog code for a constant valued current source and voltage source.
4.	Verilog-A/MS model for a junction diode and junction diode with resistors
5.	Write Verilog-A model for a linear voltage control voltage source (VCVS)
6.	Write a Verilog-A/MS model for an ideal periodic (self-clocked) sample and
7.	Write a Verilog-A/MS model that measures and saves the time interval between
8.	Write a Verilog-A/MS model for an N-bit analog-to-digital converter
9.	Write a Verilog-A/MS model for an N-bit analog-to-digital converter
10.	Write a Verilog-A/MS model for an N-bit digital-to-analog converter.

Text Books:	
1.	Behzad Razavi, Design of Analog CMOS Integrated Circuits", McGraw Hill Education Publication, 2017.
2.	Ken Kundert and Olaf Zinke, "The Designer's Guide to Verilog-AMS", Kluwer Academic Publishers.
3.	Arjuna Marzuki, "CMOS Analog and Mixed-signal Circuit Design: Practices and Innovations", 1st Edition, CRC Press, 2020.
Reference Books:	
1.	R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation, IEEE press Wiley Fourth Edition, 2019
2.	Phillip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design" Oxford University Press Second Edition.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20

marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

Laboratory- 50 Marks

Experiment Conduction with proper results is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

CO-PO-PSO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	2	2	1	-	-	-	-	-	-	1	2	2
CO2	3	3	2	2	1	-	-	-	-	-	-	1	2	2
CO3	3	3	2	2	1	-	-	-	-	-	-	1	2	2
CO4	3	3	2	2	1	-	-	-	-	-	-	1	1	1
CO5	3	3	2	2	1	-	-	-	-	-	-	1	1	1

High-3, Medium-2, Low-1

B.E. (VLSI Design and Technology)

Semester: VII		
VLSI PHYSICAL DESIGN		
Course Code:	**MVJ22VL73**	**CIE Marks:50**
Credits:	**L:T:P:S 4:0:0:Y**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Explain the fundamental concepts and techniques involved in VLSI physical design, including floorplanning, placement, routing, and timing analysis.	
2	Apply various algorithms to partition circuits and optimize floorplanning.	
3	Implement placement strategies to minimize wirelength and maximize performance.	
4	Design efficient routing and clock distribution using various algorithms.	
5	Apply techniques for optimizing the physical layout of VLSI circuits, focusing on minimizing area, power consumption, and signal delay.	

UNIT 1	
VLSI Design and Process: Introduction**,** architectural design, logic design, physical design, **Layout Styles:** Full-custom layout, gate-array layout, standard- cell layout, macro-cell layout, programmable logic arrays, FPGA layout, comparison of different design styles, difficulties in physical design, definitions and notation: Nets and netlist, connectivity information, weighted nets, grids, trees, and distances. **Laboratory Sessions/ Experimental Learning:** 1. Create and optimize layouts for custom cells using electronic design automation (EDA) tools. Verify the layout against design rules and perform layout versus schematic (LVS) checks. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc21_cs12/preview	**8Hrs.**
UNIT 2	
Circuit Partitioning and Floor planning: Circuits Partitioning: Brief details of circuit partitioning, Cost Function and Constraints: Bounded size partitions, minimize external wiring, **Approaches to Partitioning Problem:** Kernighan-Lin algorithm, variations of Kernighan-Lin algorithm, Fiduccia Mattheyses heuristic, simulated annealing.	**8Hrs.**

Floor planning: Brief introduction of floorplanning, floorplanning model, cost functions, terminologies related to floorplanning, **Approaches to Floorplanning:** Cluster growth, simulated annealing, analytical technique and dual graph technique. **Laboratory Sessions/ Experimental Learning:** 1. Analyze the impact of floorplanning on performance metrics such as wirelength, area, and power. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc21_cs12/preview 2. https://onlinecourses.nptel.ac.in/noc23_ee137/preview h	
UNIT 3	
Circuits Placement: Challenges in Placement, Cost functions and constraints, estimation of wirelength, minimize total wirelength, minimize maximum cut, minimize maximum density, maximize performance. **Approaches to Placement:** Partition-based methods, limitation of the min-cut heuristic, simulated annealing, numerical techniques, artificial neural networks and genetic algorithm. **Laboratory Sessions/ Experimental Learning:** 1. Analyze the impact of placement on performance metrics such as wirelength, timing, and congestion. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc21_cs12/preview 2. https://onlinecourses.nptel.ac.in/noc23_ee137/preview	**8Hrs.**
UNIT 4	
Routing or automated Interconnections and Clock Design: Introduction and challenges of routing **Grid Routing**: Maze routing algorithms, line search algorithms, power and ground routing and multi-layer routing. **Global Routing**: Sequential global routing, integer programming, global routing by simulated annealing, and hierarchical global routing. **Channel Routing**: Brief of channel routing, cost function and constrajnts, approaches *to* channel routing: basic left-edge algorithm, dogleg algorithm, yoshimura and kuh algorithm, greedy channel router, switchbox routing. **Clock routing and power/Ground**	**8Hrs.**

Laboratory Sessions/ Experimental Learning: 1. Perform grid routing on the imported design and analyze the initial routing results. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc21_cs12/preview 2. https://onlinecourses.nptel.ac.in/noc23_ee137/preview	
UNIT 5	
Layout Generation, Editors and Compaction: **Brief About Different Types of Layout,** Behavioral level, structural level, physical level, layout generation: standard-cells, programmable logic array. standard-cell generation and optimizations, optimization of gate-matrix layout, **Programmable Logic Arrays:** PLA personality, optimization of PLAs, capabilities of layout editors, different types of layout system, **Layout Compaction:** Compaction Algorithms, Horizontal Virtual Grid Compaction, Constraint Graph Compaction, **Real Time Logic Validations:** Integrated logic analyzer (Xilinx ILA IP) and Virtual input and output (VIO) **Laboratory Sessions/ Experimental Learning**: 1. Enter a sample combinational logic design and set up the initial PLA environment. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc21_cs12/preview	**8Hrs.**

Course Outcomes: After completing the course, the students will be able to	
CO1	Identify and explain different VLSI design styles, including their respective challenges and notation.
CO2	Apply a variety of algorithms to effectively partition VLSI circuits, ensuring balanced partitioning that meets design constraints.
CO3	Implement advanced placement strategies aimed at minimizing wirelength, thereby reducing delay and power consumption.
CO4	Design efficient routing schemes using various algorithms to ensure signal integrity and minimize delays.
CO5	Assess the trade-offs involved in physical design decisions and propose optimal solutions based on analysis and evaluation.

Text Books:	
1.	Sadiq M. Sait, and Habib Youssef, "VLSI physical design automation: theory and practice", Vol. 6. World Scientifi.
2.	Sneh Saurabh, "Introduction to VLSI design flow" Cambridge University Press, 2023.
Reference Books:	
1.	Naveed A. Sherwani, "Algorithms for VLSI physical design automation", Springer Science & Business Media, 2012.
2.	Majid S Sarrafzadeh, and C. K. Wong, "An introduction to VLSI physical design", McGraw-Hill Higher Education.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

Laboratory- 50 Marks

Experiment Conduction with proper results is evaluated for 40 marks and Viva is for 10 marks. Total SEE for laboratory is 50 marks.

CO-PO-PSO Mapping														
CO/PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**
CO2	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**
CO3	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**
CO4	**3**	**2**	**2**	**-**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**
CO5	**3**	**2**	**2**	**2**	**-**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**

High-3, Medium-2, Low-1

B.E. (VLSI Design and Technology)

Semester: VII		
ADVANCES IN VLSI DESIGN		
Course Code:	**MVJ22VL741**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**

Course Learning Objectives: The students will be able to	
1	Understand various implementation strategies for digital integrated circuits, including standard cell-based design, gate array, and full custom design.
2	Analyze the impact of interconnects on VLSI circuit performance and reliability, and develop strategies to mitigate issues such as signal delay, crosstalk, and power consumption.
3	Analyze the timing issues in digital integrated circuit (IC) design, and learn techniques to analyze, optimize, and ensure timing closure in complex digital systems.
4	Implement techniques for various memory and array structures in digital VLSI circuits, such as SRAM, DRAM, ROM, and CAM.
5	Analyze the factors affecting memory reliability and yield in VLSI design

UNIT 1	
Implementation Strategies for Digital ICs: Introduction, from custom to semicustom and structured array design approaches, custom circuit design, cell- based design methodology, standard cell, compiled cells, macrocells, megacells and intellectual property, semi-custom design flow, array-based implementation approaches, pre-diffused (or mask-programmable) arrays, pre-wired arrays **Laboratory Sessions/ Experimental Learning**: 1. Design, synthesize, and layout a digital circuit using a standard cell library. **Video Link / Additional Online Information:** **1.** https://archive.nptel.ac.in/courses/117/101/117101004/	**8Hrs.**
UNIT 2	
Coping with Interconnect: Introduction, capacitive parasitics, capacitance and reliability-cross talk, capacitance and performance in CMOS, resistive parasitics, resistance and reliability-ohmic voltage drop, electromigration, resistance and performance-RC delay,	**8Hrs.**

inductive parasitics, inductance and reliabilityvoltage drop, inductance and performance-transmission line effects **Laboratory Sessions/ Experimental Learning**: 1. Analyze and mitigate issues such as signal delay, crosstalk, and power consumption associated with VLSI interconnects. **Video Link / Additional Online Information:** **1.** https://archive.nptel.ac.in/courses/117/101/117101004/	
UNIT 3	
Timing Issues In Digital Circuits: Introduction, timing classification of digital systems, synchronous interconnect, mesochronous interconnect, plesiochronous interconnect, asynchronous interconnect, synchronous design — an in-depth perspective, synchronous timing basics, sources of skew and jitter, clock- distribution techniques, latch-base clocking, self-timed circuit design, self- timed logic - an asynchronous technique, completion-signal generation, self- timed signaling, synchronizers and arbiters, synchronizers-concept and implementation, arbiters, clock synthesis and synchronization using a phase- locked loop, basic concept, building blocks of a PLL. **Laboratory Sessions/ Experimental Learning**: 1. Understand and analyze timing issues in digital circuits and learn to identify and resolve timing violations using various techniques **Video Link / Additional Online Information:** **1.** https://archive.nptel.ac.in/courses/117/101/117101004/	**8Hrs.**
UNIT 4	
Designing Memory and Array Structures: Introduction, memory classification, memory architectures and building blocks, the memory core, read-only memories, nonvolatile read-write memories, read-write memories (RAM), contents-addressable or associative memory (CAM), memory peripheral circuitry, the address decoders, sense amplifiers, voltage references, drivers/buffers, timing and control. **Laboratory Sessions/ Experimental Learning**: 1. Design, simulate, and analyze the performance of a 6T SRAM cell. Evaluate the stability, read/write operations, and power consumption of the SRAM cell.	**8Hrs.**

Video Link / Additional Online Information: **1.** https://archive.nptel.ac.in/courses/117/101/117101004/	
UNIT 5	
Memory Reliability and Yield: Signal-to-noise ratio, memory yield, power dissipation in memories, sources of power dissipation in memories, partitioning of the memory, addressing the active power dissipation, data retention dissipation **Laboratory Sessions/ Experimental Learning**: 1. Analyze factors affecting memory reliability and yield in VLSI circuits. Implement techniques to improve memory reliability, such as error correction codes (ECC) and redundancy. **Video Link / Additional Online Information:** **1.** https://archive.nptel.ac.in/courses/117/101/117101004/	**8Hrs.**

Course Outcomes: After completing the course, the students will be able to	
CO1	Apply design automation for complex circuits using the different implementation methodology like custom versus semi-custom, hardwired versus fixed, regular array versus ad-hoc.
CO2	Utilizes the approaches to minimize the impact of interconnect parasitics on performance, power dissipation and circuit reliability
CO3	Analyze and apply synchronous, clocked approaches to impose the ordering of switching events, ensuring that desired timing constraints are met
CO4	Analyze the reliability of the memory structures
CO5	Analyze the role of peripheral circuitry such as the decoders, sense amplifiers, drivers and control circuitry in the design of reliable and fast memories.

Text Books:	
1.	Jan M Rabey, AnanthaChandrakasan, Borivoje, Digital Integrated Circuits-A Design Perspective, PHI, 2nd Edition.

Reference Books:	
1.	M. Smith, Application Specific Integrated circuits, Addison Wesley

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	2	2	1	1	1	-	1	-	-	1	1	1
CO2	3	3	2	2	1	1	1	-	1	-	-	1	1	1
CO3	3	3	2	2	1	1	1	-	1	-	-	1	1	1
CO4	3	3	2	2	1	1	1	-	1	-	-	1	1	1
CO5	3	3	2	2	1	1	1	-	1	-	-	1	1	1

High-3, Medium-2, Low-1

B.E. (VLSI Design and Technology)

Semester: VII		
MEMORY DEVICES AND CIRCUITS		
Course Code:	**MVJ22VL742**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Understand the evolution and significance of memory technologies in high-performance computing and AI/ML	
2	Analyze SRAM structures and their applications in different computing environments.	
3	Evaluate advanced DRAM designs and architectures, considering their performance and scalability.	
4	Describe various non-volatile memory types and their architectures.	
5	Address memory reliability and radiation effects, proposing strategies to mitigate potential issues in different memory technologies.	

UNIT 1	
Introduction: History of memory technologies, importance of memory technologies in high performance computing and AI/ML. Different categories of volatile and non-volatile memories **Laboratory Sessions/ Experimental Learning**: 1. Perform read and write operations on various memory devices. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/127/105/127105234/ 2. https://onlinecourses.nptel.ac.in/noc20-cs43/preview	**8Hrs.**
UNIT 2	
Volatile memories for SRAM: Static random access memories (SRAMs): SRAM cell structure- MOS SRAM architecture, MOS SRAM cell and peripheral circuit operation, bipolar SRAM technologies, silicon on insulator (SOI) technology, advanced SRAM architectures and technologies, application specific SRAMs **Laboratory Sessions/ Experimental Learning**: 1. Compare bipolar SRAM with CMOS SRAM in terms of speed, power, and area.	**8Hrs.**

Video Link / Additional Online Information: 1. https://archive.nptel.ac.in/courses/127/105/127105234/ 2. https://onlinecourses.nptel.ac.in/noc20-cs43/preview	
UNIT 3	
Volatile memories for DRAM: DRAM technology development, DRAMs cell theory and advanced cell structures, BiCMOS DRAMs-soft error failure in DRAMs, advanced DRAM designs and architecture, application specific DRAMs like GDRAM, high bandwidth memories (HBM). **Laboratory Sessions/ Experimental Learning**: 1. Create a simplified circuit model of a BiCMOS DRAM cell using CAD tools. Simulate the DRAM cell operation and introduce noise or particle effects to simulate soft errors. **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/127/105/127105234/ 2. https://onlinecourses.nptel.ac.in/noc22_ee08/preview	**8Hrs.**
UNIT 4	
Nonvolatile Memories: Masked read, only memories (ROMs): High density ROMs, programmable read-only memories (PROMs)- bipolar PROMs, CMOS PROMs, EPROM, floating Gate EPROM cell- one, time programmable (OTP) (EEPROMs), EEPROM technology and architecture, nonvolatile SRAM-Flash memories (EPROMs or EEPROM), advanced flash memory architecture, advanced non-volatile random access memories MRAM, RRAM and PC-RAMs. **Laboratory Sessions/ Experimental Learning**: 1. Understand the basic principles and operation of Programmable Read-Only Memories (PROMs). **Video Link / Additional Online Information:** 1. https://archive.nptel.ac.in/courses/127/105/127105234/ 2. https://onlinecourses.nptel.ac.in/noc22_ee08/preview	**8Hrs.**
UNIT 5	
Semiconductor Memory Reliability and Radiation Effects: General reliability issues, RAM failure modes and mechanism, non-volatile memory reliability, reliability modeling	**8Hrs.**

and failure rate prediction, design for reliability, reliability test structures, reliability screening and qualification. Radiation effects, single event phenomenon (SEP)- radiation hardening techniques, radiation hardening process and design issues, radiation-memory characteristics, radiation hardness assurance and testing, radiation dosimetry, water level radiation testing and test structures.

Laboratory Sessions/ Experimental Learning:

1. Identify common failure modes in RAM devices. Learn methods to diagnose and troubleshoot RAM failures.

Video Link / Additional Online Information:

1. https://archive.nptel.ac.in/courses/108/105/108105157/
2. https://www.digimat.in/nptel/courses/video/108105157/L15.html

Course Outcomes: After completing the course, the students will be able to	
CO1	Demonstrate an understanding of the historical development and current trends in memory technologies for high-performance computing and AI/ML applications.
CO2	Analyze different SRAM architectures, including static cell designs and associative memory structures.
CO3	Evaluate advanced DRAM technologies such as DDR, HBM, and emerging designs like STT-RAM and MRAM.
CO4	Understand nonvolatile memory types including Flash memory, EEPROM, PCM, and others, focusing on their operational principles and applications.
CO5	Address the challenges and mitigation strategies related to memory reliability.

Text Books:	
1.	Ashok K Sharna, "*Advanced Semiconductor Memories – Architecture, Design and Applications"*, Wiley publication.
2.	Yu, Shimeng. Semiconductor Memory Devices and Circuits. CRC Press, 2022.
Reference Books:	
1.	Jack Luecke, William N. Carr, "*Semiconductor Memory Design & Application*", Mc-Graw Hill.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50 =100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PS0 2**
CO1	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**
CO2	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**
CO3	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**
CO4	**3**	**2**	**2**	**-**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**2**
CO5	**3**	**2**	**2**	**2**	**-**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**2**

High-3, Medium-2, Low-1

B.E. (VLSI Design and Technology)

Semester: VII		
NANOELECTRONICS		
Course Code:	**MVJ22VL743**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Understand the fundamentals of Ideal MOS capacitor.	
2	Describe the non-idealities in MOS capacitors, such as interface traps, oxide charges, and their impact on device performance.	
3	Analyze the impact of scaling on MOSFET performance, identifying the key challenges and limitations associated with short channel effects.	
4	Evaluate the reliability issues in MOSFETs, such as hot carrier injection, negative bias temperature instability (NBTI), and time-dependent dielectric breakdown (TDDB), and propose strategies for mitigation	
5	Assess different FET structures and nano devices, comparing their advantages and limitations in terms of performance, scalability, and application potential.	

UNIT 1	
Prerequisites*: Physics of semiconductor device* **Idea MOSCAP**: Ideal MOS fundamentals, accumulation, depletion and inversion, threshold voltage, oxide and interface charges, CV characteristics of MOS, definition of technology node **Laboratory Sessions/ Experimental Learning:** 1. Measure C-V characteristics of p channel MOSFET **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117108047	**8Hrs.**
UNIT 2	
Non Ideal Effects: Impact of gate work function, oxide and interface charges, poly depletion, quantum capacitance, gate leakage, effect on C-V characteristics.	**8Hrs.**

Laboratory Sessions/ Experimental Learning: 1. MOS parameter extraction from C-V. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117108047	
UNIT 3	
Scaling Effects: MOS Scaling theory, issues in scaling MOS transistors, short channel effects, channel length modulation, drain induced barrier lowering, punch through, velocity saturation, SiO_2 vs high-k gate dielectrics. **Laboratory Sessions/ Experimental Learning:** 1. Calculate the threshold voltage of n-channel mosfet. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117108047	**8Hrs.**
UNIT 4	
MOS Transistor Reliability: Overview, negative bias temperature instability, positive bias temperature instability, substrate and gate current, hot carrier degradation, stress induced leakage current. **Laboratory Sessions/ Experimental Learning:** 1. To examine the I-V characteristics of p-channel MOSFET. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117108047	**8Hrs.**
UNIT 5	
Emerging Devices: SOI - PDSOI and FDSOI, vertical transistors - FinFET and surround gate FET. Emerging nano materials: Nanotubes, nanorods and other nano structures **Laboratory Sessions/ Experimental Learning:** 1. Draw the I-V of SOI and conventional MOSFET. **Video Link / Additional Online Information:**	**8Hrs.**

1. https://nptel.ac.in/courses/117108047	
Course Outcomes: After completing the course, the students will be able to	
CO1	Analyze the non-ideal effects in MOSCAP
CO2	Analyze the measured I-V for MOSFET that includes the scaling effects
CO3	Apply knowledge of stress and temperature effects to understand their impact on the performance of MOSFETs.
CO4	Describe the various FET device structures and their operational principles.
CO5	Analyze the performance metrics of devices based on emerging nanomaterials and structures, comparing them to conventional materials and devices to evaluate potential benefits and limitations for future nanoelectronic applications.
Text Books:	
1.	Semiconductor Device Fundamentals Book by Robert F. Pierret
Reference Books:	
1.	Fundamentals of Modern VLSI Devices, Y. Taur and T. Ning, Cambridge University Press.
2.	Silicon VLSI Technology, Plummer, Deal , Griffin , Pearson Education India.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the

entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping													
CO/PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
CO1	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**2**	**2**
CO2	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**2**	**2**
CO3	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**2**	**2**
CO4	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**2**	**2**
CO5	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**2**	**2**

High-3, Medium-2, Low-1

B.E (VLSI Design and Technology)

Semester: VII		
STATIC TIMING ANALYSIS		
Course Code:	**MVJ22VL744**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40 T**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Explain the static timing analysis (STA) environment and its key concepts, including setup and hold time, clock skew, and timing paths.	
2	Analyze interconnect parasitics, including resistance, capacitance, and inductance, and their impact on signal integrity.	
3	Illustrate the process of interconnect delay calculations, including the use of Elmore delay and other models to estimate propagation delays in interconnects.	
4	Utilize a standard cell library to identify timing models and delay models for various cells, and apply these models to calculate delays in digital circuits.	
5	Analyze the delay calculations and timing verification concepts of flip-flops, including setup and hold time analysis, and assess their impact on the overall timing closure of a digital design.	

UNIT-1	
Introduction: Nanometer designs, what is static timing analysis? why static timing analysis? crosstalk and noise, design flow, CMOS digital designs, FPGA designs, asynchronous designs, STA at different design phases **STA Concepts:** CMOS logic design, basic MOS structure, CMOS logic gate, standard cells, modeling of CMOS cells, switching waveform, propagation delay, slew of a waveform, skew between signals **Laboratory Sessions/ Experimental Learning:** 1. Analyze static timing parameters of basic gates and flipflops. **Video Link / Additional Online Information:** **1.** http://www.digimat.in/nptel/courses/video/117106109/L28.html	**8Hrs.**
UNIT-2	
Standard Cell Library: Pin capacitance, timing modeling, linear timing model, non-linear delay model, example of non-linear, delay model lookup, threshold specifications and slew derating timing models - combinational cells, delay and slew models, positive or negative unate, general combinational block, timing models - sequential cells	**8Hrs.**

Laboratory Sessions/ Experimental Learning: 1. Use standard cells to design digital circuits. Perform layout generation and design rule checking (DRC) **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc24_ee77/preview	
UNIT-3	**8Hrs.**
Interconnect Parasitics: RLC for interconnect, wireload models, interconnect trees, specifying wire load models, representation of extracted parasitic, detailed standard parasitic format, reduced standard parasitic format, standard parasitic exchange format, representing coupling capacitances **Delay Calculation:** Overview, delay calculation basics, delay calculation with interconnect, pre-layout timing, post-layout timing, cell delay using effective capacitance, interconnect delay, Elmore delay, higher order interconnect delay estimation, full chip delay calculation **Laboratory Sessions/ Experimental Learning:** 1. Analyze the delays of various basic gates and flipflops. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc24_ee77/preview	
UNIT-4	**8Hrs.**
Configuring the STA Environment: What is the STA environment? specifying clocks, clock uncertainty, clock latency, generated clocks, example of master clock at clock gating cell output, generated clock using edge and edge shift options, generated clock using invert option, clock latency for generated clocks, typical clock generation scenario **Laboratory Sessions/ Experimental Learning:** 1. For any combinational and sequential circuit, perform the configuration the STA Environment and verify the STA environment. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc24_ee77/preview	
UNIT-5	**8Hrs.**
Timing Verification: Setup timing check, flip-flop to flip-flop path, input to flip-flop path, input path with actual clock, flip flop to output path, input to output path, frequency histogram,	

hold timing check, flip-flop to flip- flop path, hold slack calculation, input to flip-flop path, flip-flop to output path, flip-flop to output path with actual clock **Laboratory Sessions/ Experimental Learning:** 1. For any combinational and sequential circuit, perform the timing verification. **Video Link / Additional Online Information:** https://onlinecourses.nptel.ac.in/noc24_ee77/preview	

Course Outcomes: After completing the course, the students will be able to	
CO1	Utilize the principles and methodologies of Static Timing Analysis (STA) tools to evaluate the timing of digital circuits.
CO2	Describe the process of calculating interconnect parasitics, including resistance, capacitance, and inductance, and discuss their effects on signal integrity and circuit timing.
CO3	Apply techniques to calculate interconnect delays, incorporating the impact of parasitics, and assess their implications for overall circuit performance.
CO4	Utilize timing and delay models from standard cell libraries to conduct precise timing analysis and optimization of digital circuits.
CO5	Analyze delay calculations for flip-flops, understanding and verifying critical timing parameters such as setup time, hold time, and clock-to-Q delay to ensure proper circuit functionality.

Text Books:	
1.	Bhasker, R Chadha, "Static Timing Analysis for Nanometer Designs: A Practical Approach", Springer Reference Books
2.	Sridhar Gangadharan, Sanjay Churiwala, "Constraining Designs for Synthesis and Timing Analysis – A Practical Guide to Synopsis Design Constraints (SDC)", Springer, 2013
Reference Books:	
1.	Naresh Maheshwari and SachinSapatnekar, "Timing Analysis and Optimization of Sequential Circuits", Springer Science and Business Media

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of

quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50 =100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PS02
CO1	3	2	2	-	-	-	-	-	-	-	-	-	2	2
CO2	3	2	2	-	-	-	-	-	-	-	-	-	2	2
CO3	3	2	2	-	-	-	-	-	-	-	-	-	2	2
CO4	3	2	2	-	2	2	-	-	-	-	-	-	1	2
CO5	3	2	2	2	-	2	-	-	-	-	-	-	1	2

High-3,Medium-2,Low-1

B.E. (VLSI Design and Technology)

Semester: VII		
VLSI DESIGN FOR SIGNAL PROCESSING		
Course Code:	**MVJ22VL751**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Explain essential DSP algorithms, including finite impulse response (FIR) and infinite impulse response (IIR) filtering, and their applications in signal processing.	
2	Apply algorithmic strength reduction techniques to digital filters and transforms, optimizing computational efficiency and resource utilization in various signal processing applications.	
3	Implement pipelining and parallel processing techniques for infinite impulse response (IIR) filters, demonstrating their effectiveness in enhancing processing speed and efficiency.	
4	Analyze and design bit-level arithmetic architectures, such as adders, multipliers, and shifters, optimizing them for performance, area efficiency, and power consumption in digital circuits.	
5	Examine the principles and implementation methodologies of synchronous wave and asynchronous pipelining techniques in digital circuit design	

UNIT 1	
Introduction to DSP systems: Typical DSP algorithms, data flow and dependence graphs - critical path, loop bound, iteration bound, longest path matrix algorithm **Pipelining and Parallel processing of FIR filters:** Pipelining and parallel processing for low power. **Laboratory Sessions/ Experimental Learning:** 1. Implement pipelining and parallel processing techniques to optimize the performance of FIR filters. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc20_ee44/preview	**8Hrs.**
UNIT 2	

Retiming – Definitions and properties, unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application **Algorithmic strength reduction in filters and transforms:** 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, odd-even merge-sort architecture, parallel rank-order filters. **Laboratory Sessions/ Experimental Learning:** 1. Implement retiming and algorithmic strength reduction techniques to optimize the performance of digital filters and transforms. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc20_ee44/preview	**8Hrs.**
UNIT 3	
Pipelining and parallel processing of IIR filters: Fast convolution – cook-toom algorithm, modified cook-toom algorithm, pipelined and parallel recursive filters – look-ahead pipelining in first-order IIR filters, look-ahead pipelining with power- of-2 decomposition, clustered look-ahead pipelining, parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters. **Laboratory Sessions/ Experimental Learning:** 1. Implement pipelining and parallel processing techniques to optimize the performance of IIR filters. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc20_ee44/preview	**8Hrs.**
UNIT 4	
Bit-level arithmetic architectures – Parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, distributed arithmetic fundamentals and FIR filters **Laboratory Sessions/ Experimental Learning:**	**8Hrs.**

1. Implement and analyze bit-level arithmetic operations using ripple carry adder (RCA) **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc20_ee44/preview	
UNIT 5	
Synchronous Wave and Asynchronous Pipelining: Numerical strength reduction – sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol. **Laboratory Sessions/ Experimental Learning:** 1. Implement and compare synchronous wave pipelining and asynchronous pipelining techniques. Analyze their performance, timing characteristics, and design considerations in digital circuitry. **Video Link / Additional Online Information:** 1. https://onlinecourses.nptel.ac.in/noc20_ee44/preview	**8Hrs.**

Course Outcomes: After completing the course, the students will be able to	
CO1	Illustrate the use of various DSP algorithms and represent them using block diagrams, signal flow graphs, and data-flow graphs, explaining the significance of each representation.
CO2	Utilize pipelining and parallel processing techniques in the design of high-speed and low-power applications, demonstrating improvements in processing efficiency and power consumption.
CO3	Apply unfolding techniques in the design of parallel architectures, showcasing how they enhance the throughput and performance of DSP systems.
CO4	Evaluate the effectiveness of look-ahead techniques in the implementation of parallel and pipelined IIR digital filters, assessing their impact on filter performance and computational efficiency.

CO5	Develop and analyze an algorithm, architecture, or circuit design for DSP applications, focusing on optimizing key metrics such as speed, power consumption, and area efficiency.

Text Books:	
1.	"VLSI Digital Signal Processing Systems", Keshab K. Parhi, Wiley Eastern
2.	Digital Signal Processing for Multimedia Systems", Keshab K. Parhi and Takao Nishitani, Marcel Dekker.
Reference Books:	
1.	"Pipelined Lattice and Wave Digital Recursive Filters", J. G. Chung and Keshab K. Parhi, Kluwer.

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

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Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	2	2	1	1	1	-	1	-	-	1	1	1
CO2	3	3	2	2	1	1	1	-	1	-	-	1	1	1
CO3	3	3	2	2	1	1	1	-	1	-	-	1	1	1
CO4	3	3	2	2	1	1	1	-	1	-	-	1	1	1
CO5	3	3	2	2	1	1	1	-	1	-	-	1	1	1

High-3, Medium-2, Low-1

B.E. (VLSI Design and Technology)

Semester: VII		
BASIC VLSI DESIGN		
Course Code:	**MVJ22VL752**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Explain the principles of MOS transistor theory and the fundamentals of CMOS technologies, including their operational characteristics and applications.	
2	Describe the various architectural choices in designing and realizing circuits in CMOS technology, emphasizing the design considerations and constraints.	
3	Apply knowledge of CMOS circuit design to evaluate performance trade-offs, such as power consumption, speed, and area, in different circuit implementations.	
4	Analyze subsystem design processes in CMOS technology, identifying key steps and techniques for optimizing the design and ensuring functionality.	
5	Demonstrate the concepts and techniques of CMOS testing, implementing testing procedures to ensure the reliability and correctness of CMOS circuits.	

UNIT 1	
Introduction: A brief history, MOS transistors, MOS transistor theory, ideal I-V characteristics, non-ideal I-V effects, DC transfer characteristics **Fabrication:** nMOS fabrication, CMOS fabrication [P-well process, N-well process, twin tub process], BiCMOS technology **Laboratory Sessions/ Experimental Learning:** 1. Measure and analyze the key characteristics of a MOS transistor, including the threshold voltage, transconductance, and the I_{DS}-V_{DS} characteristics, using SPICE simulation. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117106092	**8Hrs.**

UNIT 2	
MOS and BiCMOS Circuit Design Processes: MOS layers, stick diagrams, design rules and layout. basic circuit concepts: sheet resistance, area capacitances of layers, standard unit of capacitance, some area capacitance calculations, delay unit, inverter delays, driving large capacitive loads **Laboratory Sessions/ Experimental Learning:** 1. Design the layout of a MOS transistor using CAD tools, ensuring adherence to design rules, and simulate the electrical characteristics of the layout. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117106092	**8Hrs.**
UNIT 3	
Scaling of MOS Circuits: Scaling models & scaling factors for device parameters subsystem design processes: some general considerations, an illustration of design processes, illustration of the design processes: regularity, design of an ALU Subsystem, the Manchester Carrychain and adder enhancement techniques **Laboratory Sessions/ Experimental Learning:** 1. Understand the impact of scaling on the performance of MOS circuits by comparing key performance metrics such as threshold voltage, current drive capability, power consumption, and speed for different technology nodes using SPICE simulation. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117106092	**8Hrs.**
UNIT 4	
Subsystem Design: Some architectural issues, switch logic, gate (restoring) logic, parity generators, multiplexers, the programmable logic array (PLA) **FPGA Based Systems:** Introduction, basic concepts, digital design and FPGAs, FPGA based system design, FPGA architecture, physical design for FPGAs **Laboratory Sessions/ Experimental Learning:**	**8Hrs.**

1. To design, implement, and test a simple digital system using an FPGA. Create a 4-bit binary counter with an up/down control using VHDL/Verilog, synthesizing the design, and implementing it on an FPGA board. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117106092	
UNIT 5	
Memory, Registers and Aspects of system Timing: System timing considerations, some commonly used storage/memory elements **Testing and Verification:** Introduction, logic verification, logic verification principles, manufacturing test principles, design for testability **Laboratory Sessions/ Experimental Learning:** 1. Understand and implement testing and verification techniques for a digital system on an FPGA. Create a simle 4-bit ALU (Arithmetic Logic Unit), write testbenches for simulation, and perform in-circuit verification on an FPGA board. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117106092	**8Hrs.**
Course Outcomes: After completing the course, the students will be able to	
CO1	Demonstrate understanding of MOS transistor theory, CMOS fabrication flow, and the principles of technology scaling in semiconductor manufacturing.
CO2	Analyze memory elements in VLSI circuits, considering timing considerations such as setup time, hold time, and clock cycles, to ensure reliable operation.
CO3	Apply knowledge of FPGA-based system design to develop and implement digital systems using FPGAs for various applications.
CO4	Analyze testing and testability issues in VLSI design, evaluating methodologies and techniques to ensure comprehensive testing coverage and fault detection.
CO5	Analyze CMOS subsystems and architectural issues within the constraints of design specifications.

Text Books:	
1.	Basic VLSI Design"- Douglas A Pucknell & Kamran Eshraghian, PHI, 3rd Edition.
2.	"CMOS VLSI Design- A Circuits and Systems Perspective", Neil H E Weste, David Harris, Ayan Banerjee, 3rd Edition, Pearson Education.
3.	"FPGA Based System Design", Wayne Wolf, Pearson Education, Technology and Engineering
Reference Books:	
1.	Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations" Springer, 2011

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

CIE is executed by way of quizzes (Q), tests (T) and assignments. A minimum of three quizzes are conducted along with tests. Test portion is evaluated for 50 marks and quiz is evaluated for 10 marks. Faculty may adopt innovative methods for conducting quizzes effectively. The number of quizzes may be more than three (conduct additional quizzes and take best three). The three tests are conducted for 50 marks each and the average of all the tests are calculated for 50. The marks for the assignments are 20 (2 assignments for 10 marks each). The marks obtained in test, quiz and assignment are added to get marks out of 100 and report CIE for 50 marks.

Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

CO-PO-PSO Mapping														
CO/PO	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
CO1	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**
CO2	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**
CO3	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**
CO4	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**
CO5	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**1**	**1**

High-3, Medium-2, Low-1

B.E. (VLSI Design and Technology)

Semester: VII		
IC TECHNOLOGY		
Course Code:	**MVJ22VL753**	**CIE Marks:50**
Credits:	**L:T:P: 3:0:0**	**SEE Marks: 50**
Hours:	**40L**	**SEE Duration: 3 Hrs**
Course Learning Objectives: The students will be able to		
1	Explain the various crystal structures of semiconductors and the different methods used for semiconductor growth, including their principles and applications.	
2	Utilize the principles behind silicon dioxide oxidation and oxide charges to solve problems related to the fabrication and performance of semiconductor devices.	
3	Implement basic lithography concepts and techniques in practical scenarios, demonstrating the ability to produce patterns and structures on semiconductor wafers.	
4	Analyze the processes and outcomes of diffusion and ion implantation doping methods, comparing their effects on semiconductor properties and device performance.	
5	Evaluate metallization and etching methods in semiconductor fabrication	

UNIT 1	
Prerequisites*: Basic science* **Introduction to Microelectronics Fabrication and Crystal Growth:** Introduction and historical perspective, crystallography and crystal structure, crystal defects, Czochralski and float zone growth, sheet resistant measurement, hall measurement, basic fabrication process. **Laboratory Sessions/ Experimental Learning:** 1. To study the details regarding crystal structure. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117106093	**8Hrs.**
UNIT 2	
Thermal Oxidation: Importance of oxidation, types of oxidation techniques, growth mechanism, factors affecting	**8Hrs.**

the growth mechanisms, silicon oxidation model, dry & wet oxidation, oxide charges in Si/SiO_2 system. **Laboratory Sessions/ Experimental Learning:** 1. Measure the oxide thickness grown on Si wafer grown in dry furnace **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117106093	
UNIT 3	
Lithography: Basic concepts, optical lithography, photoresists, light sources and wafer exposure systems, optics, modulation transfer function **Laboratory Sessions/ Experimental Learning:** 1. Measure the minimum feature size of patterned Silicon using optical microscopy. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117106093	**8Hrs.**
UNIT 4	
Diffusion: Diffusion mechanisms; diffusion reactor; diffusion profile; diffusion kinetics; Dopants and their behaviors, choice of dopants **Ion Implantation:** Reactor design, impurity distribution profile, properties of ion implantation, low energy and high energy ion implantation. **Laboratory Sessions/ Experimental Learning:** 1. Measure the resistivity of doped area of wafer. **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117106093	**8Hrs.**
UNIT 5	
Deposition: Types of deposition system, thermal deposition, e-beam deposition, sputtering. **Etching**: Performance metrics of etching; types of etching- wet and dry etching; dry etching techniques.	**8Hrs.**

Laboratory Sessions/ Experimental Learning: 1. Measure the thickness of metal deposited onto the wafer **Video Link / Additional Online Information:** 1. https://nptel.ac.in/courses/117106093	

Course Outcomes: After completing the course, the students will be able to	
CO1	Describe the basic process flow of CMOS fabrication process
CO2	Analyze the factor affecting the oxide growth mechanism
CO3	Apply knowledge of VLSI fabrication principles to design and optimize mask layouts for photolithography
CO4	Analyze the dose required for given doping in diffusion and ion implantation techniques.
CO5	Explain the deposition and etching techniques

Text Books:	
1.	Silicon VLSI Technology: Fundamentals, Practice and Modeling Book by Jim Plummer, Michael D. Deal, and Peter B. Griffin
2.	The Science and Engineering of Microelectronic Fabrication by Stephen A. Campbell
Reference Books:	
1.	VLSI Fabrication Principles: Silicon and Gallium Arsenide by Sorab K. Ghandhi

Continuous Internal Evaluation (CIE):

Theory for 50 Marks

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Semester End Examination (SEE):

Total marks: 50+50=100

SEE for 50 marks is executed by means of an examination. The Question paper for each course contains two parts, Part – A and Part – B. Part – A consists of objective type questions for 20 marks covering the entire syllabus. Part – B Students have to answer five questions, one from each unit for 16 marks adding up to 80 marks. Each main question may have a maximum of three sub divisions. Each unit will have internal choice in which both questions cover entire unit having same complexity in terms of COs and Bloom's taxonomy level.

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CO1	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**2**	**2**
CO2	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**2**	**2**
CO3	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**2**	**2**
CO4	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**2**	**2**
CO5	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**-**	**1**	**-**	**-**	**1**	**2**	**2**

High-3, Medium-2, Low-1