VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

M.TECH IN ELECTRONICS & COMMUNICATION (VLSI DESIGN)

Scheme of Teaching and Examinations 2022

Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2022-23)

I SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	SDA	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	BSC	MVJ22MATEE11	Advanced Engineering Mathematics	TD:-Mathematics	03	00	00	-	03	50	50	100	3
2	IPCC	MVJ22LVL12	VLSI Design with Verilog	TD:-ECE	03	00	02	-	03	50	50	100	4
3	PCC	MVJ22LVL13	Advanced Embedded Systems	TD:-ECE	03	00	00	-	03	50	50	100	3
4	PCC	MVJ22LVL14	VLSI Testing	TD:-ECE	03	00	00	-	03	50	50	100	3
5	PCC	MVJ22LVL15	ASIC Design	TD:-ECE	03	00	00	Y	03	50	50	100	4
6	MCC	MVJ22RMI16	Research Methodology and IPR	Humanities	03	00	00	-	03	50	50	100	3
7	PCCL	MVJ22LVSL17	VLSI Design Lab-1	TD:-ECE	01	00	02	-	03	50	50	100	2
8	AUD/AEC	MVJ22AUD18	BOS recommended ONLINE courses		If the course is a Theory				00	50	50	100	0
					0	0	0						
					If a course is a laboratory				00				
					0	0	0						
Total					16	00	04	00	18	400	400	800	22

PCC: Professional Core Course, **PCCL**: Professional Core Course laboratory, **MC**: Mandatory Course (Non-credit), **AEC**: Ability Enhancement Course, **SEC**: Skill Enhancement Course, **L:** Lecture, **T**: Tutorial, **P**: Practical **S= SDA**: Skill Development Activity, **CIE**: Continuous Internal Evaluation, **SEE**: Semester End Evaluation. K : This letter in the course code indicates common to all the stream of engineering. ESC: Engineering Science Course, ETC: Emerging Technology Course, PLC: Programming Language Course

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Professional Core Course (IPCC): Refers to Professional Core Course Theory Integrated with practical of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2022-22 may please be referred.

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II SEMESTER

Sl. No	Course and Course Code		Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	PCC	MVJ22LVL21	System Verilog	TD:-ECE	02	02	00	00	03	50	50	100	3
2	IPCC	MVJ22LVL22	Design of Analog and Mixed Mode VLSI Circuits	TD:-ECE	03	00	02	00	03	50	50	100	4
3	PEC	MVJ22LVL23X	Professional Elective 1	TD:-ECE	02	00	00	Y	03	50	50	100	3
4	PEC	MVJ22LVL24X	Professional Elective 2	TD:-ECE	02	00	00	Y	03	50	50	100	3
5	MPS	MVJ22LVL25	Mini Project with Seminar	TD:-ECE	00	02	04	Y	--	100	00	100	3
6	PCCL	MVJ22LVLL26	VLSI Design Lab-2	TD:-ECE	01	00	02	00	03	50	50	100	2
7	AUD/AEC	MVJ22AUD27	Suggested ONLINE courses	TD:-ECE	If the course is Theory: 0	0	0		00	50	50	100	0
					If the course is a lab: 0	0	0		00				
				Total	10	04	08	00	15	400	300	700	**18**

Note: PCC: Professional core courses, PEC: Professional Elective Courses, IPCC-Integrated Professional Core Courses. MPS-Mini Project With Seminar; AUD/AEC; Audit Courses / Ability Enhancement Courses (Mandatory), PCCL-Professional Core Course lab,
L-Lecture, P-Practical, T/SDA-Tutorial / Skill Development Activities(Hours are for Interaction between faculty and students)

Professional Elective 1		**Professional Elective 2**	
MVJ22LVL231	Advances in VLSI Design	MVJ22LVL241	Low Power VLSI Design
MVJ22LVL232	Nano-electronics	MVJ22LVL242	SoC Design
MVJ22LVL233	Static Timing Analysis	MVJ22LVL243	VLSI Processing Technology

1 Mini Project with Seminar: This may be hands-on practice, survey report, data collection and analysis, coding, mobile app development, field visit and report

preparation, modelling of system, simulation, analysing and authenticating, case studies, etc.
CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide, if any, and a senior faculty of the department. Students can present the seminar based on the completed mini-project. Participation in the seminar by all postgraduate students of the program shall be mandatory.
The CIE marks awarded for Mini-Project work and Seminar, shall be based on the evaluation of Mini Project work and Report, Presentation skill and performance in Question and Answer session in the ratio 50:25:25. Mini-Project with Seminar shall be considered as a head of passing and shall be considered for vertical progression as well as for the award of degree. Those, who do not take-up/complete the Mini Project and Seminar shall be declared as fail in that course and have to complete the same during the subsequent semester. There is no SEE for this course.

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III SEMESTER

Sl. No	Course and Course Code		Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	SDA	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	PCC	MVJ22LVL31	CAD of Digital Systems	TD:-ECE	03	02	00	00	4	50	50	100	4
2	PEC	MVJ22LVL32X	Professional Elective 3	TD:-ECE	03	00	00	00	3	50	50	100	3
3	PEC	MVJ22LVL33X	Professional Elective 4	TD:-ECE	03	00	00	00	3	50	50	100	3
4	PROJ	MVJ22LVL34	Project Work Phase -1	TD:-ECE	00	00	06	Y	3	100	00	100	3
5	SP	MVJ22LVL35	Societal Project	TD:-ECE	00	00	06	00	3	100	00	100	3
6	INT	MVJ22LVLI36	Internship	TD:-ECE	(06 weeks Internship Completed during the intervening vacation of II and III semesters.)				3	50	50	100	4
Total					09	02	12	00	19	400	200	600	20

Professional Elective Course

MVJ22LVL321	FinFETs and Other Multi-Gate Transistors	MVJ22LVL331	Reconfigurable Computing
MVJ22LVL322	VLSI Design for Signal Processing	MVJ22LVL332	Long Term Reliability of VLSI Systems
MVJ22LVL323	Advances in Image Processing	MVJ22LVL333	CMOS RF Circuit Design

PCC: Professional Core Course, **PCCL**: Professional Core Course laboratory, **UHV**: Universal Human Value Course, **MC**: Mandatory Course (Non-credit), **AEC**: Ability Enhancement Course, **SEC**: Skill Enhancement Course, **L:** Lecture, **T**: Tutorial, **P**: Practical **S= SDA**: Skill Development Activity, **CIE**: Continuous Internal Evaluation, **SXX**: Semester End Evaluation. **K :** The letter in the course code indicates common to al the stream of engineering. **PROJ**: Project /Mini Project. **PEC**: Professional Elective Course. **SP:** Societal Project.

Professional Core Course (IPCC): Refers to Professional Core Course Theory Integrated with practicals of the same course. Credit for IPCC can be 04 and its Teaching–

Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2022-22
Project Work Phase-1: The project work shall be carried out individually. However, in case a disciplinary or interdisciplinary project requires more participants, then a group consisting of not more than three shall be permitted. Students in consultation with the guide/co-guide (if any) in disciplinary project or guides/co-guides (if any) of all departments in case of multidisciplinary projects, shall pursue a literature survey and complete the preliminary requirements of the selected Project work. Each student shall prepare a relevant introductory project document, and present a seminar. CIE marks shall be awarded by a committee comprising of HoD as Chairman, all Guide/s and co-guide/s (if any) and a senior faculty of the concerned departments. The CIE marks awarded for project work phase -1, shall be based on the evaluation of Project Report, Project Presentation skill, and performance in the Question and Answer session in the ratio of 50:25:25.
Societal Project: Students in consultation with the internal guide as well as with external guide (much preferable) shall involve in applying technology toworkout/proposing viable solutions for societal problems. CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide if any, and a senior faculty of the department. The CIE marks awarded, shall be based on the evaluation of Project Report, Project Presentation skill, and performance in the Question and Answer session in the ratio of 50:25:25. Those, who have not pursued /completed the Societal Project, shall be declared as fail in the course and have to complete the same during subsequent semester/s after satisfying the Societal Project requirements. There is no SEE (University examination) for this course.
Internship: Those, who have not pursued /completed the internship, shall be declared as fail in the internship course and have to complete the same during subsequent University examinations after satisfying the internship requirements. Internship SEE (University examination) shall be as per the University norms. CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide if any, and a senior faculty of the department. The CIE marks awarded for project work phase -1, shall be based on the evaluation of Project Report, Project Presentation skill, and performance in the Question and Answer session in the ratio of 50:25:25.
Professional Elective Courses (PEC): A professional elective (PEC) course is intended to enhance the depth and breadth of educational experience in the Engineering and Technology curriculum. Multidisciplinary courses that are added supplement the latest trend and advanced technology in the selected stream of engineering. Each group will provide an option to select one course. The minimum number of students' strengths for offering a professional elective is 10. However, this conditional shall not be applicable to cases where the admission to the program is less than 10.

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IV SEMESTER

Sl. No	Course and Course Code		Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	SDA	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	HSMC	MVJ22LVL41	Project work phase -2	ECE	00	00	08	Y	03	100	100	200	18
			Total		00	00	08	Y	03	100	100	200	18

Project Phase-2 : Students in consultation with the guide/co-guide (if any) in disciplinary project or guides/co-guides (if any) of all departments in case of multidisciplinary projects, shall continue to work of Project Work phase -1to complete the Project work. Each student / batch of students shall prepare project document, and present a seminar.

CIE marks shall be awarded by a committee comprising of HoD as Chairman, all Guide/s and co-guide/s (if any) and a senior faculty of the concerned departments. The CIE marks awarded for project work phase -2, shall be based on the evaluation of Project Report, Project Presentation skill, and performance in the Question and Answer session in the ratio of 50:25:25.

SEE shall be at the end of IV semester. Project work evaluation and Viva-Voce examination (SEE), after satisfying the plagiarism check, shall be as per the University norms.

First Semester Syllabus for VLSI Design (M.Tech.)

Course Title	Advanced Engineering Mathematics	Semester	I
Course Code	MVJ22MATEE11	CIE	50
Total No. of Contact Hours	40	SEE	50
No. of Contact Hours/week	3 (L : T : P :: 3 : 0 : 0)	Total	100
Credits	3	Exam. Duration	3 Hours

Course objective is to:

- Apply discrete and continuous probability distributions in analyzing the probability models arising in engineering field.
- Learn the mathematical formulation of linear programming problem.
- Learn the mathematical formulation of transportation problem.
- Understand the concepts of Complex variables and transformation for solving Engineering Problems.
- Learn the solutions of partial differential equations numerically.

Module-1	
Linear Algebra-I: Introduction to vector spaces and sub-spaces, definitions, illustrative example. Linearly independent and dependent vectors- Basis-definition and problems. Linear transformations-definitions. Matrix form of linear transformations-Illustrative examples **Video link / Additional online information :** 1. https://www.youtube.com/watch?v=VSz_eKdGz88 2. https://www.youtube.com/watch?v=S3e7BHBrOhk	**8Hrs.**
Module-2	
Linear Algebra-II: Computation of eigen values and eigen vectors of real symmetric matrices-Given's method. Orthogonal vectors and orthogonal bases. Gram-Schmidt orthogonalization process	**8Hrs.**

Video link / Additional online information: 1. https://www.youtube.com/watch?v=Qttf2_aPBp4 2. https://www.youtube.com/watch?v=grXn04juZ9k	
Module-3	**8Hrs.**
Calculus of Variations: Concept of functional- Eulers equation. Functional dependent on first and higher order derivatives, Functional on several dependent variables. Isoperimetric problems-variation problems with moving boundaries. **Video link / Additional online information:** 1. https://www.youtube.com/watch?v=pJs1k_nyetY 2. https://www.youtube.com/watch?v=R7tqqhnvOJc	
Module-4	**8Hrs.**
Probability Theory: Review of basic probability theory. Definitions of random variables and probability distributions, probability mass and density functions, expectation, moments, central moments, characteristic functions, probability generating and moment generating functions-illustrations. Poisson, Gaussian and Erlang distributions examples. **Video link / Additional online information :** 1. https://www.youtube.com/watch?v=dj-X4UnIXtM 2. https://www.youtube.com/watch?v=XO0gnTxzZoI	
Module-5	**8Hrs.**
Engineering Applications on Random processes: Classification. Stationary, WSS and ergodic random process. Auto-correlation function - properties, Gaussian random process. **Video link / Additional online information:** 1. https://www.youtube.com/watch?v=Omf26GtJXCI 2. https://www.youtube.com/watch?v=8OQPiSHZBz8	

Course outcomes:

CO1	Understand vector spaces, basis, linear transformations and the process of obtaining matrix of linear transformations arising in magnification and rotation of images.
CO2	Apply the technique of singular value decomposition for data compression, least square approximation in solving inconsistent linear systems
CO3	Utilize the concepts of functional and their variations in the applications of communication systems, decision theory, synthesis and optimization of digital circuits.
CO4	Learn the idea of random variables (discrete/continuous) and probability distributions in analyzing the probability models arising in control systems and system communications.
CO5	Analyze random process through parameter-dependent variables in various random processes.

Text Books:	
1.	David C.Lay, Steven R. Lay and J.J.McDonald, "Linear Algebra and its Applications", Pearson Education Ltd., 5th Edition, 2015
2.	E. Kreyszig, "Advanced Engineering Mathematics", Wiley, 10th edition, 2015
3.	Scott L.Miller, Donald G. Childers, "Probability and Random Process with application to Signal Processing", Elsevier Academic Press, 2nd Edition, 2013

CIE Assessment:
CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests - Mini Project / Case Studies (10 Marks) - Activities/Experimentations related to courses (10 Marks)
SEE Assessment:
i. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions

of 1 or 2 marks each for total of 20 marks covering the whole syllabus.

ii. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions.

iii. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	-	-	-	-	2	1	1	2
CO2	3	2	3	2	-	-	-	-	2	1	2	2
CO3	3	3	3	3	-	-	-	-	2	2	1	2
CO4	3	2	3	3	-	-	-	-	2	1	1	2
CO5	3	3	2	-	3	-	-	-	3	1	3	3

High-3, Medium-2, Low-1

Course Title	**VLSI DESIGN WITH VERILOG**	**Semester**	I
Course Code	MVJ22LVL22	**CIE**	50
Total No. of Contact Hours	40 Lecture + 10 LAB	**SEE**	50
No. of Contact Hours/week	3 (L : T : P :: 3 : 0 : 2)	**Total**	100
Credits	4	**Exam. Duration**	3 Hours

Course objective is to:

- To understand the operation of MOS transistor, Scaling and Small Geometry Effects.
- Realization of the basic IC design concepts.
- To study Static Characteristics, Switching Characteristics and Interconnect Effect of MOS Inverter.
- To provide the insight of Semiconductor Memories, Dynamic Logic Circuits and BiCMOS Logic Circuits.
- To understand basic verilog coding.

Module-1	
MOS Transistor: The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small- Geometry Effects. **MOS Inverters-Static Characteristics:** Introduction, Resistive-Load Inverter, Inverters with n_Type MOSFET Load **Laboratory Sessions/ Experimental learning:** 1. Analyze the transistor behaviour and plot VI characteristics. 2. Develop a 1st order MOSFET model using Verilog-A **Video link / Additional online information :** **1.** https://archive.nptel.ac.in/courses/108/108/108108122/ **2.** https://www.youtube.com/watch?v=Q0nhtmYT6uA	**8Hrs.**
Module-2	**8Hrs.**

MOS Inverters-Static Characteristics: CMOS Inverter. **MOS Inverters:** Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitics, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters. **Video link / Additional online information:** **1.** https://nptel.ac.in/courses/117107094 **2.** https://www.youtube.com/watch?v=K4D8zOwVNro	
Module-3	**8Hrs.**
Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM) **Basic BiCMOS Circuits:** Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications. **Video link / Additional online information:** **1.** https://www.youtube.com/watch?v=x6sj8dq1XJI **2.** https://www.youtube.com/watch?v=K5fbK6_VbtU	
Module-4	**8Hrs.**
Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS circuits **Video link / Additional online information :** **1.** https://www.youtube.com/watch?v=hwEa50roJDM **2.** https://www.youtube.com/watch?v=qt4aYyDxCOs	
Module-5	**8Hrs.**
Basics of verilog : Typical HDL-flow, why Verilog HDL?, trends in HDLs. Gate-Level Modeling: Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays.	

Behavioral Modeling: Structured procedures, initial and always, blocking and non- blocking statements, delay control, generate statement, event control, conditional statements, Multiway branching, loops, sequential and parallel blocks. **Video link / Additional online information:** **1.** https://archive.nptel.ac.in/courses/117/106/117106034/ **2.** https://avcce.digimat.in/nptel/courses/video/117106034/L06.html	

PRACTICAL COMPONENT	
1.	Write Verilog code for SR and verify the flip flop.
2.	Write Verilog code for D and verify the flip flop.
3.	Write Verilog code for JK and verify the flip flop
4.	Write Verilog code for T and verify the flip flop.
5.	Write Verilog code for MSJK and verify the flip flop.
6	Write Verilog code for counter with given input clock and check whether it works as clock divider performing division of clock by 2, 4, 8 and 16.
7	Verify the functionality of the code Model in Verilog for a full adder and add functionality to perform logical operations of XOR, XNOR, AND and OR gates. Write test bench with appropriate input patterns to verify the modeled behavior.
8	Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter with Wn = Wp, Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following: i Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and time period of 20ns and plot the input voltage and output voltage of designed inverter? ii. From the simulation results compute tpHL, tpLH and td for all three geometrical settings of width? iii Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter?
Innovative Design/Industry Related Exercise	
1.	Design and test simple 8-bit microprocessor architecture.

Course outcomes:	
CO1	Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation.
CO2	Analyse the Switching Characteristics in Digital Integrated Circuits.

CO3	Use the Dynamic Logic circuits in state-of-the-art VLSI chips.
CO4	Use Bipolar and Bi-CMOS circuits in very high speed design.
CO5	Learn verilog coding to perform digital logic design.

Text Books:	
1.	"Sung Mo Kang & Yusuf Leblebici", CMOS Digital Integrated Circuits: Analysis and Design, Tata McGraw-Hill, Third Edition.
2.	"Neil Weste and K. Eshraghian", Principles of CMOS VLSI Design: A System Perspective Pearson Education (Asia) Pvt. Ltd. Second Edition, 2000.
3.	"Douglas A Pucknell& Kamran Eshraghian", Basic VLSI Design PHI 3rd Edition
4.	Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Pearson Education, Second Edition.

CIE Assessment:

CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests

- Mini Project / Case Studies (10 Marks)
- Activities/Experimentations related to courses (10 Marks)

SEE Assessment:

i. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus.
ii. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions.
iii. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	-	-	-	-	2	1	1	2
CO2	3	3	3	2	-	-	-	-	2	1	1	2
CO3	3	2	2	3	-	-	-	-	3	1	1	2
CO4	3	3	3	3	-	-	-	-	2	1	1	2
CO5	3	2	2	-	2	-	-	-	3	1	2	3

High-3, Medium-2, Low-1

Course Title	ADVANCED EMBEDDED SYSTEMS	Semester	I
Course Code	MVJ22LVL13	CIE	50
Total No. of Contact Hours	40	SEE	50
No. of Contact Hours/week	3 (L : T : P :: 3 : 0 : 0)	Total	100
Credits	3	Exam. Duration	3 Hours

Course objective is to:

- To understand basic concepts of Embedded Systems.
- To know development of Hardware Software co-design in Embedded System.
- To understand Architecture of ARM-32 bit Microcontroller.
- To analyse Instruction sets by Assembly basics, Instruction list and description.
- To learn Cortex-M3 programming using C language concepts and Microcontroller Software Interface Standard concepts.

Module-1	
Embedded System: Embedded vs General computing system, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Opto-coupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems **Video link / Additional online information :** **1.** https://archive.nptel.ac.in/courses/108/106/108106158/ **2.** http://acl.digimat.in/nptel/courses/video/108105118/L42.html	**8Hrs.**
Module-2	
Embedded System (Continued): Hardware Software Co-Design, embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), Files generated during compilation, simulators, emulators and debugging **Video link / Additional online information:**	**8Hrs.**

1. https://nptel.ac.in/courses/108105187 **2.** https://www.youtube.com/watch?v=ail2kYwdbqc	
Module-3	**8Hrs.**
ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence . **Video link / Additional online information:** **1. https://archive.nptel.ac.in/courses/108/105/108105132/** **2. https://archive.nptel.ac.in/courses/117/106/117106114/**	
Module-4	**8Hrs.**
Instruction Sets: Assembly basics, Instruction list and description, useful instructions, **Memory Systems:** Memory maps, Memory access attributes ,Default Memory Access Permissions ,Bit band operations ,Endian Mode . **Video link / Additional online information :** **1. https://www.youtube.com/watch?v=G_sjY2jd6Kk** **2. https://www.nptelvideos.com/video.php?id=2379&c=12**	
Module-5	**8Hrs.**
Exceptions, Nested Vector interrupt controller design, Systick Timer, Cortex-M3 Programming using assembly and C language, CMSIS . **Laboratory Sessions/ Experimental learning:** 1. Design SRAM and DRAM memory using suitable VLSI tool. **Video link / Additional online information:** **1. https://www.youtube.com/watch?v=OeRk8XZnk0s** **2. https://www.youtube.com/watch?v=_eAL-v5oNOw**	

Course outcomes:	
CO1	Understand the basic hardware components and their selection method based on

	the characteristics and attributes of an embedded system.
CO2	Explain the hardware software co-design and firmware design approaches.
CO3	Understand the suitability of the instruction sets of ARM processors to design of embedded systems.
CO4	Acquire the knowledge of the architectural features of ARM CORTEX M3, a 32-bit microcontroller including memory map, interrupts and exceptions.
CO5	Able to write programs for ARM microcontroller.

Text Books:	
1.	K. V. Shibu , "Introduction to embedded systems", TMH education Pvt. Ltd. 2009
2.	Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", Newnes, (Elsevier) 2nd edn, 2010.
3.	James K. Peckol , "Embedded systems - A contemporary design tool", John Wiley, 2008

CIE Assessment:

CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests

- Mini Project / Case Studies (10 Marks)
- Activities/Experimentations related to courses (10 Marks)

SEE Assessment:

i. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus.

ii. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions.

iii. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	3	2	-	-	-	-	2	1	1	2
CO2	3	3	2	2	-	-	-	-	3	1	1	2
CO3	3	3	3	3	-	-	-	-	2	1	1	2
CO4	3	2	3	2	-	-	-	-	2	1	1	2
CO5	3	3	2	-	3	-	-	-	2	1	3	3

High-3, Medium-2, Low-1

Course Title	VLSI TESTING	Semester	I
Course Code	MVJ22LVL232	CIE	50
Total No. of Contact Hours	40	SEE	50
No. of Contact Hours/week	3 (L : T : P :: 3 : 0 : 0)	Total	100
Credits	3	Exam. Duration	3 Hours

Course objective is to:

- To understand the detection, modelling, and simulation of faults in digital circuits.
- To analyse fault diagnosis and test generation techniques for combinational logic circuits.
- To understand the designing of testable logic circuits.
- To analyse design for testability techniques.
- To understand Built-In Self Test techniques and architectures

Module-1	
Faults in digital circuits: Failures and Faults, Modeling of faults, Temporary Faults. **Logic Simulation:** Applications, Problems in simulation based design verification, types of simulation, The unknown logic values, compiled simulation, event-driven simulation, Delay models, Element evaluation, Hazard Detection, Gate-level event-driven Simulation. **Video link / Additional online information :** **1. https://archive.nptel.ac.in/courses/115/105/115105122/** **2. http://www.digimat.in/nptel/courses/video/115105122/L40.html**	**8Hrs.**
Module-2	
Test generation for Combinational Logic circuits: Fault Diagnosis of digital circuits, Test generation techniques for combinational circuits, Detection of multiple faults in Combinational logic circuits. **Video link / Additional online information:**	**8Hrs.**

1. http://acl.digimat.in/nptel/courses/video/113104106/L35.html 2. https://archive.nptel.ac.in/courses/115/106/115106127/	
Module-3	**8Hrs.**
Testable Combinational logic circuit design: Testable design of multilevel combinational circuits, Synthesis of random pattern testable combinational circuits, Path delay fault testable combinational logic design, Testable PLA design. **Video link / Additional online information:** 1. https://www.youtube.com/watch?v=ebO38bbq0_4 2. https://nptel.ac.in/courses/118104008	
Module-4	**8Hrs.**
Design of testable sequential circuits: Controllability and observability, Ad-Hoc design rules for improving testability, design of diagnosable sequential circuits, the scan-path technique for testable sequential circuit design, Level Sensitive Scan Design (LSSD), Random Access Scan Technique, Partial scan, testable sequential circuit design using Non scan Techniques, Cross check, Boundary Scan. **Video link / Additional online information :** 1. https://www.youtube.com/watch?v=9SnR3M3CIm4 2. https://archive.nptel.ac.in/courses/108/101/108101089/	
Module-5	**8Hrs.**
Built-In Self Test: Test pattern generation for BIST, Output response analysis, Circular BIST, BIST Architectures. **Video link / Additional online information:** 1. https://archive.nptel.ac.in/courses/106/105/106105161/ 2. https://www.youtube.com/watch?v=H34hLpUU9PA	

Course outcomes:	
CO1	Analyze the need for fault modelling and testing of digital circuits

CO2	Generate fault lists for digital circuits and compress the tests for efficiency
CO3	Apply the various techniques to enhance testability of combinational circuits
CO4	Apply boundary scan technique to validate the performance of digital circuits
CO5	Design built-in self-tests for complex digital circuits

Text Books:	
1.	Lala Parag K," Digital Circuit Testing and Testability New York", Academic Press 1997 .
2.	Abramovici M, Breuer M A and Friedman A "Digital Systems Testing and Testable Design" D Wiley 1994.
3.	Vishwani D Agarwal" Essential of Electronic Testing for Digital, Memory and Mixed Signal Circuits" Springer 2002.
4.	Wang, Wu and Wen Morgan" VLSI Test Principles and Architectures" Kaufmann, 2006.

CIE Assessment:

CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests

- Mini Project / Case Studies (10 Marks)
- Activities/Experimentations related to courses (10 Marks)

SEE Assessment:

iv. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus.

v. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions.

vi. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	3	-	-	-	-	2	1	1	2
CO2	3	3	2	2	-	-	-	-	2	1	1	2
CO3	2	3	3	3	-	-	-	-	3	2	1	2
CO4	3	2	3	3	-	-	-	-	2	1	1	2
CO5	3	3	2	-	3	-	-	-	3	1	2	3

High-3, Medium-2, Low-1

Course Title	ASIC DESIGN	Semester	I
Course Code	MVJ22LVL15	CIE	50
Total No. of Contact Hours	40	SEE	50
No. of Contact Hours/week	3 (L : T : P :: 3 : 0 : 0)	Total	100
Credits	4	Exam. Duration	3 Hours

Course objective is to:

- To learn ASIC methodologies and programmable logic cells to implement a function on IC.
- To learn different types of VLSI architectures used in real time applications
- To gain knowledge about pre-built logic cells used in VLSI design.
- To Analyse back-end physical design flow, including partitioning, floor-planning, placement, and routing.
- To Gain sufficient theoretical knowledge for carrying out FPGA and ASIC designs.

Module-1	
Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. **CMOS Logic:** Data path Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers. **Laboratory Sessions/ Experimental learning:** 1. Analyze static timing parameters of basic gates and flipflops. **Video link / Additional online information :** **1. https://onlinecourses.nptel.ac.in/noc24_ee77/preview** **2. http://www.digimat.in/nptel/courses/video/117106109/L28.html**	**8Hrs.**
Module-2	
ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages, library cell design.	**8Hrs.**

Programmable ASIC Logic Cells: MUX as Boolean function generators, Acted ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA:XC3000 CLB, Altera FLEX and MAX, Programmable ASIC I/O Cells: Xilinx and Altera I/O Block. **Video link / Additional online information:** **1. https://www.youtube.com/watch?v=l5a9OuyU7U8** **2. https://www.youtube.com/watch?v=bJslr4r2VCM**	
Module-3	**8Hrs.**
Low-level design entry: Schematic entry: Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, vectored instances & buses, Edit in place, attributes, Netlist screener. **ASIC Construction:** Physical Design, CAD Tools System partitioning, Estimating ASIC size. **Partitioning:** Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms. **Laboratory Sessions/ Experimental learning:** 1. Analyze the delays of various basic gates and flipflops. **Video link / Additional online information:** **1. https://www.youtube.com/watch?app=desktop&v=rK20OGJuGYc** **2. https://www.youtube.com/watch?v=q_7y09IzTdc**	
Module-4	**8Hrs.**
Floor planning and placement: Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning. **Placement:** Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow. **Laboratory Sessions/ Experimental learning:** 1. For any combinational and sequential circuit, perform the configuration the	

STA Environment and verify the STA environment. **Video link / Additional online information :** **1. https://www.youtube.com/watch?v=PR32MtwCEso** **2. https://www.youtube.com/watch?v=2dL1qt-GILE**	
Module-5	**8Hrs.**
Routing: Global Routing: Goals and objectives, Global Routing Methods, Global routing between blocks, Back- annotation. **Detailed Routing:** Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Area-Routing Algorithms, Multilevel routing, Timing –Driven detailed routing, Final routing steps, Special Routing, Circuit extraction and DRC. **Laboratory Sessions/ Experimental learning:** 1. For any combinational and sequential circuit, perform the timing verification. **Video link / Additional online information:** **1. https://www.youtube.com/watch?v=m86zSu8vbZE** **2. https://www.youtube.com/watch?v=QBv2Mno3mwE**	

Course outcomes:	
CO1	Describe the concepts of ASIC design methodology, data path elements, logical effort.
CO2	Analyze the design of ASICs suitable for specific tasks, perform design entry and explain the physical design flow
CO3	Design data path elements for ASIC cell libraries and compute optimum path delay.
CO4	Create floor plan including partition and routing with the use of CAD algorithms.
CO5	Design CAD algorithms and explain how these concepts interact in ASIC design.

Text Books:	
1.	Michael John Sebastian Smith, "Application - Specific Integrated Circuits", Addison- Wesley Professional, 2005

2.	Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations" Springer, ISBN: 978-1-4614-1119-2. 2011
3.	Rakesh Chadha, Bhasker J, "An ASIC Low Power Primer", Springer, ISBN: 978-14614-4270-7.

CIE Assessment:

CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests

- Mini Project / Case Studies (10 Marks)
- Activities/Experimentations related to courses (10 Marks)

SEE Assessment:

vii. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus.

viii. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions.

ix. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2	2	-	-	-	-	3	1	1	2
CO2	3	3	3	2	-	-	-	-	2	1	1	2
CO3	3	2	3	3	-	-	-	-	2	2	1	2
CO4	3	3	3	3	-	-	-	-	2	1	1	2
CO5	3	3	3	-	3	-	-	-	2	1	3	3

High-3, Medium-2, Low-1

Course Title	**RESEARCH METHODOLOGY AND IPR**	**Semester**	II
Course Code	MVJ22RMI16	**CIE**	50
Total No. of Contact Hours	40	**SEE**	50
No. of Contact Hours/week	3 (L : T : P :: 3 : 0 : 0)	**Total**	100
Credits	3	**Exam. Duration**	3 Hours

Course objective is to:

- To give an overview of the research methodology and explain the technique of defining a research problem
- To explain the details of sampling designs, and also different methods of data collections.
- To explain the art of interpretation and the art of writing research reports.
- To explain various forms of the intellectual property, its relevance and business impact in the changing global business environment.
- To discuss leading International Instruments concerning Intellectual Property Rights

Module-1	
Research Methodology: Introduction, Meaning of Research, Objectives of Research, Types of Research,Research Approaches, Significance of Research, Research Methods versus Methodology, Research and Scientific Method, Research Process, Criteria of Good Research, Problems Encountered by Researchers in India. **Defining the Research Problem:** Research Problem, Selecting the Problem, Necessity of Defining the Problem,Technique Involved in Defining a Problem, An Illustration. **Video link / Additional online information :** **1.** **https://www.youtube.com/watch?v=TFOO1JAll2Y** **2.** **https://www.youtube.com/watch?v=nmLw3ONx8L8**	**8Hrs.**

Module-2	
Reviewing the literature: Place of the literature review in research, Bringing clarity and focus to research problem, Improving research methodology, Broadening knowledge base in research area, Enabling contextual findings, Review of the literature, searching the existing literature, reviewing the selected literature, Developing a theoretical framework, Developing a conceptual framework, Writing about the literature reviewed. **Video link / Additional online information:** **1.** **https://www.youtube.com/watch?v=TIdMKf7jR70** **2.** **https://www.youtube.com/watch?v=ij1Joifi1to**	**8Hrs.**
Module-3	**8Hrs.**
Design of Sample Surveys: Design of Sampling: Introduction, Sample Design, Sampling and Non-sampling Errors, Sample Survey versus Census Survey, Types of Sampling Designs. **Measurement and Scaling:** Qualitative and Quantitative Data, Classifications of Measurement Scales, Goodness of Measurement Scales, Sources of Error in Measurement, Techniques of Developing Measurement Tools, Scaling, Scale Classification Bases, Scaling Technics, Multidimensional Scaling, Deciding the Scale. **Data Collection:** Introduction, Experimental and Surveys, Collection of Primary Data, Collection of Secondary Data, Selection of Appropriate Method for Data Collection, Case Study Method. **Video link / Additional online information:** **1.** **https://www.youtube.com/watch?v=_A7fUR2Itsc** **2.** **https://www.youtube.com/watch?v=mwklBb6RvNs**	
Module-4	
Testing of Hypotheses: Hypothesis, Basic Concepts Concerning Testing of Hypotheses, Testing of Hypothesis, Test Statistics and Critical Region, Critical Value and Decision Rule, Procedure for Hypothesis Testing, Hypothesis Testing	**8Hrs.**

for Mean, Proportion, Variance, for Difference of Two Mean, for Difference of Two Proportions, for Difference of Two Variances, P-Value approach, Power of Test, Limitations of the Tests of Hypothesis. **Chi-square Test:** Test of Difference of more than Two Proportions, Test of Independence of Attributes, Test of Goodness of Fit, Cautions in Using Chi Square Tests. **Video link / Additional online information :** **1. http://acl.digimat.in/nptel/courses/video/106105034/L17.html** **2. http://acl.digimat.in/nptel/courses/video/106105034/L29.html**	
Module-5	
Interpretation and Report Writing: Meaning of Interpretation, Technique of Interpretation, Precaution in Interpretation, Significance of Report Writing, Different Steps in Writing Report, Layout of the Research Report, Types of Reports, Oral Presentation, Mechanics of Writing a Research Report, Precautions for Writing Research Reports. **Intellectual Property:** The Concept, Intellectual Property System in India, Development of TRIPS Complied. **Video link / Additional online information:** **1. https://www.youtube.com/watch?v=6XTYoZymbwE** **2. https://www.youtube.com/watch?v=X8bDsfO4Lf8**	**8Hrs.**

Course outcomes:	
CO1	Illustrate research problem formulation
CO2	Analyse research related information and research ethics
CO3	Summarize the present day scenario controlled and monitored by Computer and Information Technology, where the future world will be ruled by dynamic ideas, concept, creativity and innovation.
CO4	Explain how IPR would take such important place in growth of individuals & nation, to summarize the need of information about Intellectual Property Right

	to be promoted among student community in general & engineering in particular.
CO5	Relate that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about economic growth and social benefits.

Text Books:	
1.	C.R. Kothari and Gaurav Garg, "Research Methodology: Methods and Techniques" , New Age International Publications, 4th Edition
2.	Ranjit Kumar, "Research Methodology a step-by step guide for beginners", SAGE Publications, 3rd Edition
3.	N.K.Acharya, "Intellectual Property Rights", Asia Law House, 6th Edition

CIE Assessment:

CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests

- Mini Project / Case Studies (10 Marks)
- Activities/Experimentations related to courses (10 Marks)

SEE Assessment:

i. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus.
ii. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions.
iii. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	-	-	-	-	2	1	1	2
CO2	3	3	3	2	-	-	-	-	2	1	1	2
CO3	3	3	3	3	-	-	-	-	2	1	1	2
CO4	3	3	3	3	-	-	-	-	2	1	1	2
CO5	3	3	2	-	3	-	-	-	3	1	3	3

High-3, Medium-2, Low-1

Course Title	VLSI Design Lab-I	Semester	I
Course Code	MVJ22LVSL17	CIE	50
Total No. of Contact Hours	14 (LAB)	SEE	50
No. of Contact Hours/week	3 (L : T : P :: 0 : 0 : 2)	Total	100
Credits	2	Exam. Duration	3 Hours

Course objective is to:

- Familiarize with the CAD tool (Xilinx ISE/Vivado) to write HDL programs.
- Understand simulation and synthesis of digital design.
- Program FPGAs/CPLDs to synthesize the digital designs.
- Interface hardware to programmable ICs through I/O ports.
- Choose either Verilog or VHDL for a given Abstraction level.

Sl. No.	Experiments
1	Write Verilog code for the 4-bit counter [Synchronous & Asynchronous counter].
2	Write Verilog code for the design of 8-bit Carry Ripple Adder
3	Write Verilog code for the design of 8-bit Carry Look Ahead adder
4	Write Verilog code for the design of 8-bit Carry Skip Adder
5	Magnitude Comparator Array Multiplication (Signed and Unsigned)
6	Magnitude Comparator Booth Multiplication (Radix-4)
7	Write Verilog code for 4/8-bit Magnitude Comparator
8	Write Verilog code for 4/8-bit LFSR.
9	Write Verilog code for 4/8-bit Parity Generator
10	Write Verilog code for 4/8-bit Universal Shift Register
11	Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence. Eg 11101 (with and without overlap) any sequence can be specified.

Course outcomes:	
CO1	Write the Verilog programs to simulate Combinational circuits in Dataflow, Behavioral and Gate level Abstractions.
CO2	Describe sequential circuits like flip flops and counters in Behavioral

	description and obtain simulation waveforms.
CO3	Synthesize Combinational and Sequential circuits on programmable ICs and test the hardware.
CO4	Interface the hardware to the programmable chips and obtain the required output
CO5	Verify the design using a logic analyzer

CIE Assessment:
CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests - Mini Project / Case Studies (10 Marks) - Activities/Experimentations related to courses (10 Marks)
SEE Assessment:
i. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus. ii. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions. iii. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	-	-	-	-	2	1	1	2
CO2	3	3	3	2	-	-	-	-	2	1	1	2
CO3	3	3	3	3	-	-	-	-	2	1	1	2
CO4	3	3	3	3	-	-	-	-	2	1	1	2
CO5	3	3	2	-	3	-	-	-	3	1	3	3

High-3, Medium-2, Low-1

Second Semester Syllabus for VLSI Design (M.Tech.)

Course Title	SYSTEM VERILOG	Semester	II
Course Code	MVJ22LVL21	CIE	50
Total No. of Contact Hours	40	SEE	50
No. of Contact Hours/week	3 (L : T : P :: 3 : 0 : 0)	Total	100
Credits	3	Exam. Duration	3 Hours

Course objective is to:

- To understand the concepts of Verification process.
- To know the concepts of System Verilog.
- To gain the essential knowledge to write the Verification Code.
- To learn Randomization of system Verilog.
- To examine functional coverage depending upon data sample

Module-1	
Verification Guidelines: The verification process, basic test bench functionality, directed testing, methodology basics, constrained random stimulus, randomization, functional coverage, test bench components, layered testbench. **Video link / Additional online information :** 1. https://www.youtube.com/watch?v=m86zSu8vbZE 2. https://www.youtube.com/watch?v=M5SG8HaFrzc	**8Hrs.**
Module-2	
Data Types: Built in Data types, fixed and dynamic arrays, Queues, associative arrays, linked lists, array methods, choosing a storage type, creating new types with typedef, creating user defined structures, type conversion, Enumerated types, constants and strings, Expression width **Video link / Additional online information:** 1. https://www.youtube.com/watch?v=U18k9TDP5uw	**8Hrs.**

2. https://www.youtube.com/watch?v=YiM9fYsc8lk	
Module-3	**8Hrs.**
Connecting the test bench and design: Separating the test bench and design, The interface construct, Stimulus timing, Interface driving and sampling, System Verilog assertions. **Video link / Additional online information:** **1. http://www.digimat.in/nptel/courses/video/106105165/L01.html** **2. https://www.youtube.com/watch?v=foe9HDtp9y0**	
Module-4	**8Hrs.**
Randomization: Introduction, Randomization in System Verilog, Constraint details, Solution probabilities, Valid constraints, Inline constraints, Random number functions, Common randomization problems **Laboratory Sessions/ Experimental learning:** 1. Create random data using system verilog for testing dual port memory architecture. **Video link / Additional online information :** **1. https://www.youtube.com/watch?v=PauVSWup6Sw** **2. https://www.youtube.com/watch?v=2vA7H8y8OKo**	
Module-5	**8Hrs.**
Functional Coverage: Coverage types, Coverage strategies, Simple coverage example, Anatomy of Cover group and Triggering a Cover group, Data sampling, Cross coverage, Generic Cover groups, Coverage options, Analyzing coverage data, measuring coverage statistics during simulation. **Laboratory Sessions/ Experimental learning:** 1. Test the functional coverage of dual port memory using system verilog. **Video link / Additional online information:** **1. https://www.youtube.com/watch?v=5m6_zBDB1vg** **2. https://www.youtube.com/watch?v=zLZRwOkGLNA**	

Course outcomes:	
CO1	Apply the System Verilog concepts to verify the design.
CO2	Understand the datatypes of System Verilog
CO3	Apply constrained random tests benches using System Verilog.
CO4	Understand Randomization
CO5	Appreciate Functional Coverage.

Text Books:	
1.	Chris Spear, "System Verilog for Verification – A guide to learning the Test bench language features", Springer Publications Second Edition, 2010.
2.	Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for Design-A guide to using system Verilog for Hardware design and modelling", Springer Publications Second Edition, 2006.

CIE Assessment:

CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests

- Mini Project / Case Studies (10 Marks)
- Activities/Experimentations related to courses (10 Marks)

SEE Assessment:

i. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus.

ii. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions.

iii. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	-	-	-	-	2	1	1	2
CO2	3	3	3	2	-	-	-	-	2	1	1	2
CO3	3	3	3	3	-	-	-	-	2	1	1	2
CO4	3	3	3	3	-	-	-	-	2	1	1	2
CO5	3	3	2	-	3	-	-	-	3	1	3	3

High-3, Medium-2, Low-1

Course Title	**DESIGN OF ANALOG AND MIXED MODE VLSI CIRCUITS**	**Semester**	II
Course Code	MVJ22LVL22	**CIE**	50
Total No. of Contact Hours	40 Lecture + 10 LAB	**SEE**	50
No. of Contact Hours/week	3 (L : T : P :: 3 : 0 : 2)	**Total**	100
Credits	4	**Exam. Duration**	3 Hours

Course objective is to:

- To understand the basic physics and operation of MOS devices.
- To study Single-Stage and Differential Amplifiers.
- To learn Data Converter Specifications and Architectures.
- To understand Single ended Differential Amplifier and operations.
- To learn architecture of Data converter includes ADC (Analog to Digital) and DAC(Digital to Analog) Converters

Module-1	
Basic MOS Device Physics: General considerations, MOS I/V Characteristics, second order effects, MOS device models, brief introduction of modeling of MOS and Verilog-A. **Laboratory Sessions/ Experimental learning:** 1. Analyze the transistor behaviour and plot VI characteristics. 2. Develop a 1st order MOSFET model using Verilog-A **Video link / Additional online information :** **1.** https://archive.nptel.ac.in/courses/108/108/108108122/ **2.** https://www.youtube.com/watch?v=Q0nhtmYT6uA	**8Hrs.**
Module-2	
Single stage Amplifier: Basic Concepts, Common Source stage, Source follower. **Differential Amplifiers:** Single ended and differential operation, Basic differential pair, Common mode response, Differential pair with MOS loads,	**8Hrs.**

Gilbert cell. **Video link / Additional online information:** **1.** https://nptel.ac.in/courses/117107094 **2.** https://www.youtube.com/watch?v=K4D8zOwVNro	
Module-3	**8Hrs.**
Operational Amplifiers: One Stage OP-Amp. Two Stage OP-Amp, Gain boosting, Common Mode Feedback, Slew rate, Power Supply Rejection, Noise in Op Amps. **Oscillators and Phase Locked Loops:** Ring Oscillators, LC Oscillators, VCO, Mathematical Model of VCO. Simple PLL. **Video link / Additional online information:** **1.** https://www.youtube.com/watch?v=x6sj8dq1XJI **2.** https://www.youtube.com/watch?v=K5fbK6_VbtU	
Module-4	**8Hrs.**
Oscillators and Phase Locked Loops (Continuation): Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications. **Bandgap Refernces and Switched capacitor Circuits:** General Considerations, Supply Independent biasing, PTAT Current Generation, Constant Gm Biasing, Sampling Switches, Switched Capacitor Amplifiers. **Video link / Additional online information :** **1.** https://www.youtube.com/watch?v=hwEa50roJDM **2.** https://www.youtube.com/watch?v=qt4aYyDxCOs	
Module-5	**8Hrs.**
Data Converter Architectures: DAC & ADC Specifications, Current Steering DAC, Charge Scaling DAC, Flash ADC, Successive Approximation ADC. **Video link / Additional online information:** **1.** https://archive.nptel.ac.in/courses/117/106/117106034/ **2.** https://avcce.digimat.in/nptel/courses/video/117106034/L06.html	

PRACTICAL COMPONENT	
1.	Design an Inverter with given specifications*, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) Transient Analysis b. Draw the Layout and verify the DRC, ERC d. Extract RC and back annotate the same and verify the Design e. Verify & Optimize for Time, Power and Area to the given Constraint
2.	Design the common source amplifier with given specifications, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) AC Analysis iii) Transient Analysis b. Draw the Layout and verify the DRC, ERC, LVS d. Extract RC and back annotate the same and verify the Design
3.	Design the common drai amplifier with given specifications, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) AC Analysis iii) Transient Analysis b. Draw the Layout and verify the DRC, ERC, LVS d. Extract RC and back annotate the same and verify the Design
4.	Design the Single Stage differential amplifier with given specifications, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) AC Analysis iii) Transient Analysis b. Draw the Layout and verify the DRC, ERC, LVS d. Extract RC and back annotate the same and verify the Design
5.	8-bit Operational amplifier
6.	8-bit R2R DAC

Course outcomes:

CO1	Use efficient analytical tools for quantifying the behavior of basic circuits by inspection.
CO2	Design high-performance, amplifier circuits with the trade-offs between speed, precision and power dissipation.
CO3	Design and study the behavior of phase-locked-loops for the applications.
CO4	Identify the critical parameters that affect the analog and mixed-signal VLSI circuits' performance
CO5	Perform calculations in the digital or discrete time domain, more sophisticated data converters to translate the digital data to and from inherently analog world.

Text Books:	
1.	"Behzad Razavi", Design of Analog CMOS Integrated Circuits, TMH 2007.
2.	"R. Jacob Baker", CMOS Circuit Design, Layout, and Simulation, Wiley Second Edition
3.	"Phillip E. Allen, Douglas R. Holberg", CMOS Analog Circuit Design Oxford University Press Second Edition.

CIE Assessment:

CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests

- Mini Project / Case Studies (10 Marks)
- Activities/Experimentations related to courses (10 Marks)

SEE Assessment:

i. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus.

ii. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions.

iii. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	-	-	-	-	2	1	1	2
CO2	3	3	3	2	-	-	-	-	2	1	1	2
CO3	3	3	3	3	-	-	-	-	2	1	1	2
CO4	3	3	3	3	-	-	-	-	2	1	1	2
CO5	3	3	2	-	3	-	-	-	3	1	3	3

High-3, Medium-2, Low-1

Course Title	**ADVANCES IN VLSI DESIGN**	**Semester**	II
Course Code	MVJ22LVL231	**CIE**	50
Total No. of Contact Hours	40	**SEE**	50
No. of Contact Hours/week	3 (L : T : P :: 3 : 0 : 0)	**Total**	100
Credits	3	**Exam. Duration**	3 Hours

Course objective is to:

- To understand Implementation strategies for digital ICS from custom to semi-custom Array Design.
- To know performance parameters of CMOS circuits,
- To learn Timing issues of digital system.
- To learn Timing issues of Memory design.
- To learn Timing issues of Programmable logic device (PLD).

Module-1	
Implementation Strategies For Digital ICS: Introduction, From Custom to Semicustom and Structured Array Design Approaches, Custom Circuit Design, Cell-Based Design Methodology, Standard Cell, Compiled Cells, Macrocells, Megacells and Intellectual Property, Semi-Custom Design Flow, Array-Based Implementation Approaches, Pre-diffused (or Mask-Programmable) Arrays, Pre-wired Arrays, Perspective-The Implementation Platform of the Future. **Video link / Additional online information :** **1.** https://archive.nptel.ac.in/courses/108/106/108106158/ **2.** http://acl.digimat.in/nptel/courses/video/108105118/L42.html	**8Hrs.**
Module-2	
Coping With Interconnect: Introduction, Capacitive Parasitics, Capacitance and Reliability-Cross Talk, Capacitance and Performance in CMOS, Resistive Parasitics, Resistance and Reliability-Ohmic Voltage Drop, Electromigration, Resistance and Performance-RC Delay, Inductive Parasitics, Inductance and	**8Hrs.**

Reliability- Voltage Drop, Inductance and Performance-Transmission Line Effects, Advanced Interconnect Techniques,Reduced- Swing Circuits, Current-Mode Transmission Techniques, Perspective: Networks-on-a-Chip. **Video link / Additional online information:** **1.** https://nptel.ac.in/courses/108105187 **2.** https://www.youtube.com/watch?v=ail2kYwdbqc	
Module-3	**8Hrs.**
Timing Issues In Digital Circuits: Introduction, Timing Classification of Digital Systems, Synchronous Interconnect, Mesochronous interconnect, Plesiochronous Interconnect, Asynchronous Interconnect, Synchronous Design — An In-depth Perspective, Synchronous Timing Basics, Sources of Skew and Jitter, Clock-Distribution Techniques, Latch-Base Clocking, Self-Timed Circuit Design, Self-Timed Logic - An Asynchronous Technique, Completion-Signal Generation, Self-Timed Signaling, Practical Examples of Self- Timed Logic, Synchronizers and Arbiters, Synchronizers-Concept and Implementation, Arbiters, Clock Synthesis and Synchronization Using a Phase-Locked Loop, Basic Concept, Building Blocks of a PLL. **Video link / Additional online information:** **1.** **https://archive.nptel.ac.in/courses/108/105/108105132/** **2.** **https://archive.nptel.ac.in/courses/117/106/117106114/**	
Module-4	**8Hrs.**
Designing Memory and Array Structures: Introduction, Memory Classification, Memory Architectures and Building Blocks, The Memory Core, Read-Only Memories, Nonvolatile Read-Write Memories, Read-Write Memories (RAM), Contents-Addressable or Associative Memory (CAM), Memory Peripheral Circuitry, The Address Decoders, Sense Amplifiers, Voltage References,Drivers/Buffers, Timing and Control. **Video link / Additional online information :**	

1. https://www.youtube.com/watch?v=G_sjY2jd6Kk **2. https://www.nptelvideos.com/video.php?id=2379&c=12**	
Module-5	
Designing Memory and Array Structures: Memory Reliability and Yield, Signal-to-Noise Ratio, Memory yield, Power Dissipation in Memories, Sources of Power Dissipation in Memories, Partitioning of the memory, Addressing the Active Power Dissipation, Data retention dissipation, Case Studies in Memory Design: The Programmable Logic Array (PLA), A 4Mbit SRAM, A 1 Gbit NAND Flash Memory, Perspective: Semiconductor Memory Trends and Evolutions. **Laboratory Sessions/ Experimental learning:** 1. Design SRAM and DRAM memory using suitable VLSI tool. **Video link / Additional online information:** **1. https://www.youtube.com/watch?v=OeRk8XZnk0s** **2. https://www.youtube.com/watch?v=_eAL-v5oNOw**	**8Hrs.**

Course outcomes:	
CO1	Apply design automation for complex circuits using the different implementation methodology like custom versus semi-custom, hardwired versus fixed, regular array versus ad-hoc.
CO2	Use the approaches to minimize the impact of interconnect parasitics on performance, power dissipation and circuit reliability
CO3	Impose the ordering of the switching events to meet the desired timing constraints using synchronous, clocked approach.
CO4	Infer the reliability of the memory
CO5	Understand the role of peripheral circuitry such as the decoders, sense amplifiers, drivers and control circuitry in the design of reliable and fast memories

Text Books:	
1.	Jan M Rabey, AnanthaChandrakasan, Borivoje Nikolic, "Digital Integrated

	Circuits-A Design Perspective", PHI, 2nd Edition
2.	M. Smith, "Application Specific Integrated circuits", Addison Wesley, 1997
3.	Wang, Wu and Wen, "VLSI Test Principles and Architectures", Morgan Kaufmann, 2006
4.	H. Veendrick, "MOS ICs: From Basics to ASICs", Wiley-VCH, 1992

CIE Assessment:

CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests

- Mini Project / Case Studies (10 Marks)
- Activities/Experimentations related to courses (10 Marks)

SEE Assessment:

i. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus.
ii. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions.
iii. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	-	-	-	-	2	1	1	2
CO2	3	3	3	2	-	-	-	-	2	1	1	2
CO3	3	3	3	3	-	-	-	-	2	1	1	2
CO4	3	3	3	3	-	-	-	-	2	1	1	2
CO5	3	3	2	-	3	-	-	-	3	1	3	3

High-3, Medium-2, Low-1

Course Title	NANO-ELECTRONICS	Semester	II
Course Code	MVJ22LVL232	CIE	50
Total No. of Contact Hours	40	SEE	50
No. of Contact Hours/week	3 (L : T : P :: 3 : 0 : 0)	Total	100
Credits	3	Exam. Duration	3 Hours

Course objective is to:

- To understand Overview of physics behind Nano science and engineering.
- To understand the characterization of semiconductor nanostructures.
- To learn Quantum confinement in semiconductor nanostructures.
- To analyze different fabrication process and physical process.
- To understand various types of methods of measuring properties and applications of Nanoelectronics

Module-1	
Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moores' law and continued miniaturization, Classification of Nanostructures, **Electronic properties of atoms and solids:** Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices,Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems **Video link / Additional online information :** 1. https://archive.nptel.ac.in/courses/115/105/115105122/ 2. http://www.digimat.in/nptel/courses/video/115105122/L40.html	**8Hrs.**
Module-2	
Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction	**8Hrs.**

techniques, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectrometry, Techniques for property Measurement: mechanical, electron, magnetic, thermal properties **Video link / Additional online information:** **1.** **http://acl.digimat.in/nptel/courses/video/113104106/L35.html** **2.** **https://archive.nptel.ac.in/courses/115/106/115106127/**	
Module-3	**8Hrs.**
Inorganic semiconductor nanostructures: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, and electronic density of states. **Carbon Nanostructures**: Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes. **Video link / Additional online information:** **1.** **https://www.youtube.com/watch?v=ebO38bbq0_4** **2.** **https://nptel.ac.in/courses/118104008**	
Module-4	**8Hrs.**
Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, colloidal quantum dots, self-assembly techniques. **Video link / Additional online information :** **1.** **https://www.youtube.com/watch?v=9SnR3M3CIm4** **2.** **https://archive.nptel.ac.in/courses/108/101/108101089/**	
Module-5	**8Hrs.**
Physical processes: modulation doping, quantum hall effect, resonant	

tunneling, charging effects, ballistic carrier transport, Inter band absorption, intra band absorption, Light emission processes, phonon bottleneck, quantum Confined stark effect, nonlinear effects, coherence and dephasing, **characterization of semiconductor nanostructures:** optical electrical and structural **Video link / Additional online information:** **1.** **https://archive.nptel.ac.in/courses/106/105/106105161/** **2.** **https://www.youtube.com/watch?v=H34hLpUU9PA**	

Course outcomes:	
CO1	Know the principles behind Nanoscience engineering and Nanoelectronics.
CO2	Apply the knowledge to prepare and characterize nanomaterials.
CO3	Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.
CO4	Design the process flow required to fabricate state of the art transistor technology.
CO5	Analyze the requirements for new materials and device structure in the future.

Text Books:	
1.	Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, "Nanoscale Science and Technology", John Wiley, 2007
2.	Charles P Poole, Jr, Frank J Owens, "Introduction to Nanotechnology", John Wiley Copyright 2006, Reprint 2011.
3.	Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, "Hand Book of Nanoscience Engineering and Technology", CRC press, 2003.

CIE Assessment:

CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests

- Mini Project / Case Studies (10 Marks)
- Activities/Experimentations related to courses (10 Marks)

SEE Assessment:

iv. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus.

v. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions.

vi. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	-	-	-	-	2	1	1	2
CO2	3	3	3	2	-	-	-	-	2	1	1	2
CO3	3	3	3	3	-	-	-	-	2	1	1	2
CO4	3	3	3	3	-	-	-	-	2	1	1	2
CO5	3	3	2	-	3	-	-	-	3	1	3	3

High-3, Medium-2, Low-1

Course Title	**STATIC TIMING ANALYSIS**	**Semester**	II
Course Code	MVJ22LVL233	**CIE**	50
Total No. of Contact Hours	40	**SEE**	50
No. of Contact Hours/week	3 (L : T : P :: 3 : 0 : 0)	**Total**	100
Credits	3	**Exam. Duration**	3 Hours

Course objective is to:

- To understand the STA Environment and concepts.
- To understand the interconnect parasitics calculations.
- To understand the interconnect delay calculations.
- To know standard cell library with timing model and delay model.
- To study delay calculations and timing verification concepts of flip-flops

Module-1	
Introduction: Nanometer Designs, What is Static Timing Analysis? Why Static Timing Analysis?, Crosstalk and Noise, Design Flow, CMOS Digital Designs, FPGA Designs, Asynchronous Designs, STA at Different Design Phases, Limitations of Static Timing Analysis, Power Considerations, Reliability Considerations **STA Concepts:** CMOS Logic Design, Basic MOS Structure, CMOS Logic Gate, Standard Cells, Modeling of CMOS Cells, Switching Waveform, Propagation Delay, Slew of a Waveform, Skew between Signals, Timing Arcs and Unateness, Min and Max Timing Paths, Clock Domains, Operating Conditions **Laboratory Sessions/ Experimental learning:** 1. Analyze static timing parameters of basic gates and flipflops. **Video link / Additional online information :** **1. https://onlinecourses.nptel.ac.in/noc24_ee77/preview** **2. http://www.digimat.in/nptel/courses/video/117106109/L28.html**	**8Hrs.**
Module-2	**8Hrs.**
Standard Cell Library: Pin Capacitance, Timing Modeling, Linear Timing Model,	

Non-Linear Delay Model, Example of Non-Linear, Delay Model Lookup, Threshold Specifications and Slew Derating Timing Models - Combinational Cells, Delay and Slew Models, Positive or Negative Unate, General Combinational Block, Timing Models - Sequential Cells, Synchronous Checks: Setup and Hold, Example of Setup and Hold Checks, Negative Values in Setup and Hold Checks, Asynchronous Checks, Recovery and Removal Checks Pulse Width Checks, Example of Recovery, Removal and Pulse Width Checks, Propagation Delay, State- Dependent Models XOR,XNOR and Sequential Cells, Interface Timing Model for a Black Box, Advanced Timing Modeling, Receiver Pin Capacitance, Specifying Capacitance at the Pin Level, Specifying Capacitance at the Timing Arc Level, Output Current, Models for Crosstalk Noise Analysis, DC Current, Output Voltage, Propagated Noise, Noise Models for Two-Stage Cells, Noise Models for Multi-stage and sequential Cells, Other Noise Models, Power Dissipation Modeling, Active Power **Video link / Additional online information:** **1. https://www.youtube.com/watch?v=l5a9OuyU7U8** **2. https://www.youtube.com/watch?v=bJslr4r2VCM**	
Module-3	**8Hrs.**
Interconnect Parasitics: RLC for Interconnect, Wireload Models, Interconnect Trees, Specifying Wire load Models, Representation of Extracted Parasitic, Detailed Standard Parasitic Format ,Reduced Standard Parasitic Format, Standard Parasitic Exchange Format, Representing Coupling Capacitances, Hierarchical Methodology, Block Replicated in Layout, Reducing Parasitic for Critical Nets, Reducing Interconnect Resistance, Increasing Wire Spacing, Parasitics for Correlated Nets. **Delay Calculation:** Overview, Delay Calculation Basics, Delay Calculation with Interconnect, Pre-layout Timing, Post-layout Timing, Cell Delay using Effective Capacitance, Interconnect Delay, Elmore Delay, Higher Order Interconnect Delay Estimation, Full Chip Delay Calculation, Slew Merging, Different Slew Thresholds, Different Voltage Domains, Path Delay Calculation, Combinational Path Delay,	

Path to a Flip-flop, Input to Flip-flop Path, Flip-flop to Flip-flop Path, Multiple Paths, Slack Calculation. **Laboratory Sessions/ Experimental learning:** 1. Analyze the delays of various basic gates and flipflops. **Video link / Additional online information:** **1. https://www.youtube.com/watch?app=desktop&v=rK20OGJuGYc** **2. https://www.youtube.com/watch?v=q_7y09IzTdc**	
Module-4	**8Hrs.**
Configuring the STA Environment: What is the STA Environment? Specifying Clocks, Clock Uncertainty, Clock Latency, Generated Clocks, Example of Master Clock at Clock Gating Cell Output, Generated Clock using Edge and Edge shift Options, Generated Clock using Invert Option, Clock Latency for Generated Clocks, Typical Clock Generation Scenario, Constraining Input Paths, Constraining Output Paths, Example A, Example B, Example Timing Path Groups, Modeling of External Attributes,Modeling Drive Strengths, Modeling Capacitive Load, Design Rule Checks, Virtual Clocks **Laboratory Sessions/ Experimental learning:** 1. For any combinational and sequential circuit, perform the configuration the STA Environment and verify the STA environment. **Video link / Additional online information :** **1. https://www.youtube.com/watch?v=PR32MtwCEso** **2. https://www.youtube.com/watch?v=2dL1qt-GILE**	
Module-5	**8Hrs.**
Timing Verification: Setup Timing Check, Flip-flop to Flip-flop Path, Input to Flip-flop Path, Input Path with Actual Clock, Flip flop to Output Path, Input to Output Path, Frequency Histogram, Hold Timing Check, Flip-flop to Flip- flop Path, Hold Slack Calculation, Input to Flip-flop Path, Flip-flop to Output Path, Flip-flop to Output Path with Actual Clock, Input to Output Path, Multicycle Paths, Crossing Clock Domains, False Paths, Half- Cycle Paths, Removal Timing Check,	

Recovery Timing Check, Timing across Clock Domains, Slow to Fast Clock Domains, Fast to Slow Clock Domains, Half-cycle Path - Case 1, Half-cycle Path -Case 2, Fast to Slow Clock Domain, Slow to Fast Clock **Laboratory Sessions/ Experimental learning:** 1. For any combinational and sequential circuit, perform the timing verification. **Video link / Additional online information:** **1. https://www.youtube.com/watch?v=m86zSu8vbZE** **2. https://www.youtube.com/watch?v=QBv2Mno3mwE**	

Course outcomes:	
CO1	Evaluate the delay of any given digital circuits.
CO2	Prepare the resources to perform the static timing analysis using EDA tool.
CO3	Prepare timing constraints for the design based on the specification.
CO4	Generate the timing analysis report using EDA tool for different checks.
CO5	Perform verification and analyse the generated report to identify critical issues and bottleneck for the violation and suggest the techniques to make the design to meet timing

Text Books:	
1.	Bhasker, R Chadha, "Static Timing Analysis for Nanometer Designs: A Practical Approach", Springer 2009 Reference Books
2.	Sridhar Gangadharan, Sanjay Churiwala, "Constraining Designs for Synthesis and Timing Analysis – A Practical Guide to Synopsis Design Constraints (SDC)", Springer, 2013
3.	Naresh Maheshwari and SachinSapatnekar, "Timing Analysis and Optimization of Sequential Circuits", Springer Science and Business Media, 1999

CIE Assessment:

CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests

- Mini Project / Case Studies (10 Marks)
- Activities/Experimentations related to courses (10 Marks)

SEE Assessment:

vii. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus.

viii. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions.

ix. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	-	-	-	-	2	1	1	2
CO2	3	3	3	2	-	-	-	-	2	1	1	2
CO3	3	3	3	3	-	-	-	-	2	1	1	2
CO4	3	3	3	3	-	-	-	-	2	1	1	2
CO5	3	3	2	-	3	-	-	-	3	1	3	3

High-3, Medium-2, Low-1

Course Title	**LOW POWER VLSI DESIGN**	**Semester**	II
Course Code	MVJ22LVL241	**CIE**	50
Total No. of Contact Hours	40	**SEE**	50
No. of Contact Hours/week	3 (L : T : P :: 3 : 0 : 0)	**Total**	100
Credits	3	**Exam. Duration**	3 Hours

Course objective is to:

- To study State-of-the art approaches of power estimation.
- To study different power reduction techniques.
- To study circuit level power estimation and minimization.
- To learn optimization techniques that involve reduction of power dissipation of digital circuits.
- To understand power dissipation at various levels of design.

Module-1	
Introduction: Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS leakage current, static current, basic principles of low power design, low power figure of merits. **Simulation power analysis:** SPICE circuit simulation, Monte Carlo simulation. **Laboratory Sessions/ Experimental learning:** 1. Plot the charging and discharging characteristics of capacitor using SPICE simulator. **Video link / Additional online information :** **1. https://www.youtube.com/watch?v=TFOO1JAll2Y** **2. https://www.youtube.com/watch?v=nmLw3ONx8L8**	**8Hrs.**
Module-2	
Circuit: Transistor and gate sizing, equivalent pin ordering, network restructuring and reorganization, special latches and flip flops, low power digital cell library, adjustable device threshold voltage.	**8Hrs.**

Video link / Additional online information: **1. https://www.youtube.com/watch?v=TIdMKf7jR70** **2. https://www.youtube.com/watch?v=ij1Joifi1to**	
Module-3	**8Hrs.**
Logic: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. **Low power Clock Distribution:** Power dissipation in clock distribution, single driver Vs distributed buffers. **Video link / Additional online information:** **1. https://www.youtube.com/watch?v=_A7fUR2Itsc** **2. https://www.youtube.com/watch?v=mwklBb6RvNs**	
Module-4	**8Hrs.**
Low power Architecture & Systems: Power & performance management, switching activity reduction, flow graph transformation. **Low power memory design:** Introduction, sources and reductions of power dissipation in memory subsystem. **Video link / Additional online information :** **1. http://acl.digimat.in/nptel/courses/video/106105034/L17.html** **2. http://acl.digimat.in/nptel/courses/video/106105034/L29.html**	
Module-5	**8Hrs.**
Algorithm & Architectural Level Methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis. **Advanced Techniques:** Adiabatic computation, Asynchronous circuits. **Laboratory Sessions/ Experimental learning:** 1. Optimize any given simple circuit (digital) using spice tool. **Video link / Additional online information:**	

1. https://www.youtube.com/watch?v=6XTYoZymbwE 2. https://www.youtube.com/watch?v=X8bDsfO4Lf8	

Course outcomes:	
CO1	Identify the sources of power dissipation in CMOS circuits.
CO2	Perform power analysis using simulation-based approaches and probabilistic analysis.
CO3	Use optimization and trade-off techniques that involve power dissipation of digital circuits.
CO4	Make the power design a reality by making power dimension an integral part of the design process.
CO5	Use practical low power design techniques and their analysis at various levels of design abstraction and analyse how these are being captured in the latest design automation environments.

Text Books:	
1.	Gary K. Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic, 1998.
2.	Jan M. Rabaey, Massoud Pedram, "Low Power Design Methodologies", Kluwer Academic, 2010.
3.	Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000
4.	P. Chandrasekaran and R. W. Broadersen, "Low power digital CMOS design", Kluwer Academic,1995.
5.	A Bellamour and M I Elmasri, "Low power VLSI CMOS circuit design", Kluwer Academic,1995.

CIE Assessment:
CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests

during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests

- Mini Project / Case Studies (10 Marks)
- Activities/Experimentations related to courses (10 Marks)

SEE Assessment:

iv. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus.

v. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions.

vi. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	-	-	-	-	2	1	1	2
CO2	3	3	3	2	-	-	-	-	2	1	1	2
CO3	3	3	3	3	-	-	-	-	2	1	1	2
CO4	3	3	3	3	-	-	-	-	2	1	1	2
CO5	3	3	2	-	3	-	-	-	3	1	3	3

High-3, Medium-2, Low-1

Course Title	SoC DESIGN	Semester	II
Course Code	MVJ22LVL242	CIE	50
Total No. of Contact Hours	40	SEE	50
No. of Contact Hours/week	3 (L : T : P :: 3 : 0 : 0)	Total	100
Credits	3	Exam. Duration	3 Hours

Course objective is to:

- To Describe the organization and implementation of the 3- and 5-stage pipeline ARM processor cores
- To Understand the needs high-level language (in this case, C) in application development
- To Know the issues involved in debugging systems in embedded processor cores and in the production testing of board-level systems.
- To learn different ARM integer cores, concept of memory hierarchy and management
- To Describe the organization and implementation of the 3- and 5-stage pipeline ARM processor cores

Module-1	
ARM Organization and Implementation: 3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution, ARM implementation, The ARM co-processor interface. **The ARM Instruction Set:** Introduction, Exceptions, Conditional execution, Branch and Branch with Link (B, BL), Branch, Branch with Link and exchange (BX, BLX), Software Interrupt (SWI). **Laboratory Sessions/ Experimental learning:** 1. Write simple addition, subtraction, multiplication and division program using any ARM microcontroller simulation tool. **Video link / Additional online information :** **1. http://digimat.in/nptel/courses/video/106105193/L09.html**	**8Hrs.**

2. http://www.digimat.in/nptel/courses/video/117106111/L01.html	
Module-2	**8Hrs.**
The ARM Instruction Set (Continued): Data processing instructions, Multiply instructions, Count leading zeros (CLZ - architecture v5T only), Single word and unsigned byte data transfer instruction, Half-word and signed byte data transfer instructions, Multiple register transfer instructions, Swap memory and register instructions (SWP), Status register to general register transfer instructions, General register to status register transfer instructions, Coprocessor instructions, Coprocessor data operations, Coprocessor data transfers, Coprocessor register transfers, Breakpoint instruction (BRK - architecture v5T only), Unused instruction space, Memory faults, ARM architecture **Video link / Additional online information:** **1. https://www.youtube.com/watch?v=UdY5RkkT7bg** **2. https://www.youtube.com/watch?v=l7w5HCCtQ30**	
Module-3	**8Hrs.**
Architectural Support for High-Level Languages: Abstraction in software design, Data types, Floating-point data types, The ARM floating-point architecture, Expressions, Conditional statements, Loops, Functions and procedures, Use of memory, Run-time environment. **Laboratory Sessions/ Experimental learning:** 1. Write some simple simple programs using C programming language any ARM microcontroller simulation tool. **Video link / Additional online information:** **1. https://www.digimat.in/nptel/courses/video/106105193/L07.html** **2. https://www.youtube.com/watch?v=3OmyM4-zuQw**	
Module-4	**8Hrs.**
Architectural Support for System Development: The ARM memory interface, The Advanced Microcontroller Bus Architecture(AMBA), The ARM reference peripheral specification, Hardware system prototyping tools, The ARMulator, The	

JTAG boundary scan test architecture, The ARM debug architecture, Embedded Trace, Signal processing support. **Video link / Additional online information :** **1. https://www.youtube.com/watch?v=CuuIBvHrvtA** **2. http://www.digimat.in/nptel/courses/video/106105193/L05.html**	
Module-5	**8Hrs.**
ARM Processor Cores: ARM7TDMI, ARM8, ARM9TDMI, ARM10TDMI, Discussion, Example and exercises. Memory Hierarchy: Memory size and speed, On-chip memory, Caches, Cache design - an example, Memory management, Examples and exercises **Laboratory Sessions/ Experimental learning:** 1. Write a program to interface simple ADC and DAC for real time applications. **Video link / Additional online information:** **1. https://www.youtube.com/watch?v=4VRtujwa_b8** **2. https://www.youtube.com/watch?v=JPfG0UQd3x4**	

Course outcomes:	
CO1	Apply the 3 and 5-stage pipeline ARM processor cores and analyse the implementation isses
CO2	Use the concepts and methodologies employed in designing a System- on-chip (SoC) based around a microprocessor core and in designing the microprocessor core itself.
CO3	Understand how SoCs and microprocessors are designed and used, and why a modern processor is designed the way that it is.
CO4	Use integrated ARM CPU cores (including Strong ARM) that incorporate full support for memory management.
CO5	Analyze the requirements of a modern operating system and use the ARM architecture to address the same

Text Books:	
1.	Steve Furber "ARM System-On-Chip Architecture" Addison Wesley, 2nd edition
2.	Joseph Yiu "The Definitive Guide to the ARM Cortex-M3", Newnes, (Elsevier) , 2nd edition, 2010.
3.	Sudeep Pasricha and Nikil Dutt," On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers, 2008.
4.	Michael Keating, Pierre Bricaud "Reuse Methodology Manual for System on Chip designs", Kluwer Academic Publishers, 2ndedition, 2008.

CIE Assessment:

CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests

- Mini Project / Case Studies (10 Marks)
- Activities/Experimentations related to courses (10 Marks)

SEE Assessment:

vii. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus.

viii. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions.

ix. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	-	-	-	-	2	1	1	2
CO2	3	3	3	2	-	-	-	-	2	1	1	2
CO3	3	3	3	3	-	-	-	-	2	1	1	2

CO4	3	3	3	3	-	-	-	-	2	1	1	2
CO5	3	3	2	-	3	-	-	-	3	1	3	3

High-3, Medium-2, Low-1

Course Title	**VLSI PROCESSING TECHNOLOGY**	**Semester**	II
Course Code	MVJ22LVL243	**CIE**	50
Total No. of Contact Hours	40	**SEE**	50
No. of Contact Hours/week	3 (L : T : P :: 3 : 0 : 0)	**Total**	100
Credits	3	**Exam. Duration**	3 Hours

Course objective is to:

- To understand the theoretical and practical aspect of very large scale integration
- To analyse doping profiles and material properties with SOI technology.
- To learn the art of lithography with different techniques.
- To analyse plasma discharge properties and the diagnostic techniques.
- To understand implantation process and applicability of metallization scheme.

Module-1	
Crystal Growth and Wafer Preparation: Introduction, Electronic-Grade Silicon, Czochralski Crystal Growing. **Epitaxy:** Introduction, Vapour-Phase Epitaxy. **Video link / Additional online information :** 1. https://www.youtube.com/watch?v=VSz_eKdGz88 2. https://www.youtube.com/watch?v=S3e7BHBrOhk	**8Hrs.**
Module-2	
Lithography: Introduction, Optical Lithography, Electron Lithography, X-ray Lithography, Ion Lithography. **Video link / Additional online information:** 1. https://www.youtube.com/watch?v=Qttf2_aPBp4 2. https://www.youtube.com/watch?v=grXn04juZ9k	**8Hrs.**
Module-3	**8Hrs.**
Reactive Plasma Etching: Introduction, Plasma Properties, Feature-Size	

Control and Anisotropic Etch Mechanisms, Other Properties of Etch Processes, Reactive Plasma-Etching Techniques and Equipment, Specific Etch Processes. **Video link / Additional online information:** 1. https://www.youtube.com/watch?v=pJs1k_nyetY 2. https://www.youtube.com/watch?v=R7tqqhnvOJc	
Module-4	**8Hrs.**
Ion Implantation: Introduction, Range Theory, Implantation Equipment, Annealing, Shallow Junctions, High-Energy Implantation. **Video link / Additional online information :** 1. https://www.youtube.com/watch?v=dj-X4UnIXtM 2. https://www.youtube.com/watch?v=XO0gnTxzZoI	
Module-5	**8Hrs.**
Metallization: Introduction, Metallization Applications, Metallization Choices, Physical Vapor Deposition, Patterning, Metallization problems . **Video link / Additional online information:** 1. https://www.youtube.com/watch?v=Omf26GtJXCI 2. https://www.youtube.com/watch?v=8OQPiSHZBz8	

Course outcomes:	
CO1	Understand the major steps in the fabrication process of VLSI circuits
CO2	Illustrate particular processing steps in achieving required parameters.
CO3	Apply standard engineering for different lithographic methods.
CO4	Analyse the specific plasma process used in semiconductor industry
CO5	Apply implantation process for VLSI devices and discuss the limitations of various metallization schemes.

Text Books:	
1.	"S. M. Sze, "VLSI Technology", McGraw-Hill, Second Edition.

2.	S.K. Ghandhi, "VLSI Fabrication Principles", John Wiley Inc., New York, 1994, Second Edition.

CIE Assessment:

CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests

- Mini Project / Case Studies (10 Marks)
- Activities/Experimentations related to courses (10 Marks)

SEE Assessment:

i. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus.

ii. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions.

iii. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	-	-	-	-	2	1	1	2
CO2	3	3	3	2	-	-	-	-	2	1	1	2
CO3	3	3	3	3	-	-	-	-	2	1	1	2
CO4	3	3	3	3	-	-	-	-	2	1	1	2
CO5	3	3	2	-	3	-	-	-	3	1	3	3

High-3, Medium-2, Low-1

Course Title	VLSI Design Lab-II	Semester	II
Course Code	MVJ22LVLL26	CIE	50
Total No. of Contact Hours	40	SEE	50
No. of Contact Hours/week	3 (L : T : P :: 0 : 0 : 2)	Total	100
Credits	2	Exam. Duration	3 Hours

Course objective is to:

- Understand the features of CAD tool (Cadence/Xilinx Vivado/Modelsim etc.) in VLSI design.
- Design and verify the behavior of digital circuits using digital flow
- Synthesize the circuit in VLSI tool
- Verify the design using a logic analyzer
- Analyse physical design

Sl. No.	Experiments
1	Design and test basic gates using system Verilog and calculate the coverage.
2	Design and test 1-bit full-adder circuit using system Verilog and calculate the coverage.
3	Design and test flip-flops (D, T, JK, SR and MSJK) using system Verilog and calculate the coverage.
4	Design and test synchronous FIFO using system Verilog and calculate the coverage.
5	Design and test 16-bit up-down counter circuit using system Verilog and calculate the coverage.
6	Design and test single port simple RAM using system Verilog and calculate the coverage.
7	Design and test single port simple RAM using UVM and calculate the coverage.
	Innovative Design/Industry Related Exercise
8	Verification of basic communication protocol (I2C, SPI and UART) verification using system Verilog and UVM technique.
9	Verification of basic AXI bus protocol verification using system Verilog and UVM technique.

Course outcomes:

CO1	Understand the features of CAD tool in VLSI design.
CO2	Design and verify the behavior of digital circuits using digital flow
CO3	Synthesize the circuit in VLSI tool
CO4	Verify the design using a logic analyzer
CO5	Analyse physical design

CIE Assessment:

CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests

- Mini Project / Case Studies (10 Marks)
- Activities/Experimentations related to courses (10 Marks)

SEE Assessment:

x. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus.

xi. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions.

xii. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	-	-	-	-	2	1	1	2
CO2	3	3	3	2	-	-	-	-	2	1	1	2
CO3	3	3	3	3	-	-	-	-	2	1	1	2
CO4	3	3	3	3	-	-	-	-	2	1	1	2
CO5	3	3	2	-	3	-	-	-	3	1	3	3

High-3, Medium-2, Low-1

Third Semester Syllabus for VLSI Design (M.Tech.)

Course Title	CAD OF DIGITAL SYSTEMS	Semester	III
Course Code	MVJ22LVL31	CIE	50
Total No. of Contact Hours	40	SEE	50
No. of Contact Hours/week	3 (L : T : P :: 3 : 0 : 0)	Total	100
Credits	3	Exam. Duration	3 Hours

Course objective is to:

- To understand the basic physics and operation of MOS devices.
- To study Single-Stage and Differential Amplifiers.
- To learn Data Converter Specifications and Architectures.
- To understand Single ended Differential Amplifier and operations.
- To learn architecture of Data converter includes ADC (Analog to Digital) and DAC(Digital to Analog) Converters.

Module-1	
Introduction to Design Methodologies: The VLSI Design Problem, The Design Domains, Design Actions, Design Methods and Technologies. **VLSI Design Automation tools:** Algorithmic and System Design, Structural and Logic Design, Transistor- level Design, Layout Design, Verification Methods. **Algorithmic graph theory and computational complexity:** Terminology, Data Structures for the Representation of Graphs, Computational Complexity, Examples of Graph Algorithms. **Video link / Additional online information :** 1. https://www.youtube.com/watch?v=ZOXJH-87iBA 2. https://www.youtube.com/watch?v=E--lTG9mehI	**8Hrs.**
Module-2	
Tractable and intractable problems: Decision Problems, Complexity Classes, NP-completeness and NP-hardness,	**8Hrs.**

General purpose methods for combinational optimization: Backtracking and Branch-and-bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu Search, Genetic Algorithms, A Few Final Remarks on General-purpose Methods. **Video link / Additional online information:** **1. https://archive.nptel.ac.in/courses/106/105/106105161/** **2. https://onlinecourses.nptel.ac.in/noc21_cs12/preview**	
Module-3	**8Hrs.**
Layout compaction: Design Rules, Symbolic Layout, Problem Formulation, Algorithms for Constraint-graph Compaction, Other Issues. **Placement and partitioning:** Circuit Representation, Wire-length Estimation, Types of Placement Problem, Placement Algorithm, Partitioning. **Floor planning:** Floor planning Concepts, Shape Functions and Floorplan Sizing **Video link / Additional online information:** **1. https://www.digimat.in/nptel/courses/video/106105161/L22.html** **2. https://terna.digimat.in/nptel/courses/video/106105161/L21.html**	
Module-4	**8Hrs.**
Routing: Types of Local Routing Problems, Area Routing, Channel Routing, Introduction to Global Routing, Algorithms for Global Routing. **Simulation:** General Remarks on VlSl Simulation, Gate-level Modeling and Simulation, Switch-level Modeling and Simulation **Video link / Additional online information :** 1. https://www.youtube.com/watch?v=iOmqgewj5XI 2. https://in.mathworks.com/learn/tutorials/simulink-onramp.html **3.** https://www.halvorsen.blog/documents/teaching/courses/matlab/matlab3.php	
Module-5	**8Hrs.**
Logic Synthesis and Verification: Introduction to Combinational Logic	

Synthesis, Binary-decision Diagrams, Twolevel Logic Synthesis **High level synthesis:** Hardware Models for High Level Synthesis, Internal Representation of the Input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithm, Some Aspects of the Assignment Problem, High-level Transformations **Video link / Additional online information:** **1. https://archive.nptel.ac.in/courses/117/106/117106034/** **2. https://www.nptelvideos.com/course.php?id=585**	

Course outcomes:	
CO1	Understand the various design methodologies.
CO2	Solve graph theoretic problems.
CO3	Evaluate the computational complexity of an algorithm.
CO4	Write algorithms for VLSI Automation
CO5	Simulate and synthesize digital circuits using VLSI automation tools

Text Books:	
1.	S H Gerez, "Algorithms for VLSI Design Automation", Wiley, India, 2 nd Edition
2.	N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Springer International edition, 3rd Edition

CIE Assessment:
CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests - Mini Project / Case Studies (10 Marks) - Activities/Experimentations related to courses (10 Marks)

SEE Assessment:

i. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus.

ii. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions.

iii. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	-	-	-	-	2	1	1	2
CO2	3	3	3	2	-	-	-	-	2	1	1	2
CO3	3	3	3	3	-	-	-	-	2	1	1	2
CO4	3	3	3	3	-	-	-	-	2	1	1	2
CO5	3	3	2	-	3	-	-	-	3	1	3	3

High-3, Medium-2, Low-1

Course Title	**FINFETS AND OTHER MULTI-GATE TRANSISTORS**	**Semester**	III
Course Code	MVJ22LVL321	**CIE**	50
Total No. of Contact Hours	40	**SEE**	50
No. of Contact Hours/week	3 (L : T : P :: 3 : 0 : 0)	**Total**	100
Credits	3	**Exam. Duration**	3 Hours

Course objective is to:

- To learn the evolution of SOI MOS transistor.
- To have an insight into thin film formation techniques and advanced gate stack deposition.
- To enable the students to analyse physics behind BSIM-CMG.
- To analyse the electrostatics of the multi-gate MOS system.
- To realize the interrelationship between the multi-gate FET device properties and digital and analog circuits

Module-1	
The SOI MOSFET: From Single Gate to MultiGate: brief history of Multiple - Gate MOSFETs, MultiGate MOSFET physics. **Video link / Additional online information :** **1. https://www.youtube.com/watch?v=_h6CSuwWqYg** **2. http://www.digimat.in/nptel/courses/video/117108047/L20.html**	**8Hrs.**
Module-2	
Multigate MOSFET Technology : Introduction, Active Area:Fins, Gate Stack **Video link / Additional online information:** **1. https://digimat.in/nptel/courses/video/117106093/L34.html** **2. https://archive.nptel.ac.in/courses/108/101/108101089/**	**8Hrs.**
Module-3	**8Hrs.**
IM-CMG: A Compact Model for Mult-Gate Transistors : Introduction,	

Framework for MultiGate FET Modeling, MultiGate Models, BSIM-CMG and BSIM-IMG, BSIM-CMG. **Video link / Additional online information:** **1. https://archive.nptel.ac.in/courses/117/106/117106149/** **2. https://www.digimat.in/nptel/courses/video/117101004/L01.html**	
Module-4	**8Hrs.**
Physics of the MultiGate MOS system : Device electrostatics, Double gate MOS system, Two-dimensional confinement. **Video link / Additional online information :** **1. https://archive.nptel.ac.in/courses/117/107/117107149/** **2. https://archive.nptel.ac.in/courses/115/102/115102014/**	
Module-5	**8Hrs.**
Multi-Gate MOSFET circuit Design : Introduction, Digital Circuit Design, Analog Circuit Design. **Video link / Additional online information:** **1. https://archive.nptel.ac.in/courses/108/105/108105132/** **2. https://archive.nptel.ac.in/courses/108/102/108102112/**	

Course outcomes:	
CO1	List out the advantages and challenges of Multi-gate Fin FETs.
CO2	Describe thin film formation technique.
CO3	Describe gate stack deposition technique.
CO4	Describe physics beyond BSIM- CMG.
CO5	Analyse electrostatics of multi-gate MOS system and corelate multigate FET device properties and elementary digital and analog circuits.

Text Books:	
1.	J.P.Colinge: FinFETs and other Multi-Gate Transistors, springer, Series on

	Integrated Circuits and Systems
2.	Samar Saha : Fin FET Devices for VLSI Circuits and Systems, CRC Press, First Edition, 2020
3.	Weihua Han,Zhiming M. Wang, : Toward Quantum FinFET , Springer Cham, First Edition 2021.
4.	Yogesh singh Chauhan, Darsen D, et.al , FinFET Modeling for IC Simulation and Design: using the BSIM-CMG standard, Academic Press, 2015.

CIE Assessment:

CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests

- Mini Project / Case Studies (10 Marks)
- Activities/Experimentations related to courses (10 Marks)

SEE Assessment:

iv. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus.

v. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions.

vi. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	-	-	-	-	2	1	1	2
CO2	3	3	3	2	-	-	-	-	2	1	1	2
CO3	3	3	3	3	-	-	-	-	2	1	1	2
CO4	3	3	3	3	-	-	-	-	2	1	1	2
CO5	3	3	2	-	3	-	-	-	3	1	3	3

High-3, Medium-2, Low-1

Course Title	VLSI DESIGN FOR SIGNAL PROCESSING	Semester	III
Course Code	MVJ22LVL322	CIE	50
Total No. of Contact Hours	40	SEE	50
No. of Contact Hours/week	3 (L : T : P :: 3 : 0 : 0)	Total	100
Credits	3	Exam. Duration	3 Hours

Course objective is to:

- To learn the Transformations for high speed design using pipelining, retiming, and parallel processing techniques
- To understand the Power reduction transformations for supply voltage reduction as well as for strength or capacitance reduction
- To analyse area reduction using folding techniques
- To create Strategies for arithmetic implementation
- To create Strategies for arithmetic implementation

Module-1	
Introduction to DSP Systems: Typical DSP Algorithms, DSP Application Demands and Scaled CMOS Technologies, Representations of DSP Algorithms. **Iteration Bounds:** Data flow graph Representations, loop bound and Iteration bound. Algorithms for Computing Iteration Bound, Iteration Bound of multi rate data flow graphs. **Video link / Additional online information :** **1. https://archive.nptel.ac.in/courses/108/105/108105157/** **2. https://www.digimat.in/nptel/courses/video/108105157/L15.html**	**8Hrs.**
Module-2	
Pipelining and Parallel Processing: pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power. **Retiming:** Definition and Properties, Solving Systems of Inequalities, Retiming Techniques.	**8Hrs.**

Video link / Additional online information: **1. http://acl.digimat.in/nptel/courses/video/108105118/L26.html** **2. https://www.digimat.in/nptel/courses/video/108105157/L15.html**	
Module-3	**8Hrs.**
Unfolding: An Algorithm for Unfolding, Properties of Unfolding, Critical path, Unfolding and Retiming, Application of Unfolding. **Folding:** Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding of Multirate Systems. **Video link / Additional online information:** **1. https://www.digimat.in/nptel/courses/video/108105157/L19.html** **2. https://onlinecourses.nptel.ac.in/noc24_ee63/preview**	
Module-4	**8Hrs.**
Systolic Architecture Design: systolic array design Methodology, FIR systolic array, Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D systolic Array Design, Systolic Design for space representation containing Delays. **Fast convolution:** Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution, cyclic convolution Design of fast convolution Algorithm by Inspection. **Laboratory Sessions/ Experimental learning:** 1. Design systolic array using HDL and simulate it using any HDL simulator. **Video link / Additional online information :** **1. https://nptel.ac.in/courses/108106149** **2. https://www.digimat.in/nptel/courses/video/108106149/L97.html**	
Module-5	**8Hrs.**
Pipelined and Parallel Recursive and Adaptive Filter: Pipeline Interleaving in Digital Filter, first order IIR digital Filter, Higher order IIR digital Filter, parallel processing for IIR filter, Combined pipelining and parallel processing for IIR Filter, Low power IIR Filter Design Using Pipelining and parallel processing,	

pipelined adaptive digital filter. **Laboratory Sessions/ Experimental learning:** **1.** Design and test FIR filter used for DSP applications using HDL. **2.** Design and test IIR filter used for DSP applications using HDL. **Video link / Additional online information:** **1.** **https://onlinecourses.nptel.ac.in/noc20_ee44/preview** **2.** **http://www.digimat.in/keyword/117.html**	

Course outcomes:	
CO1	Illustrate the use of various DSP algorithms and addresses their representation using block diagrams, signal flow graphs and data-flow graphs
CO2	Use pipelining and parallel processing in design of high-speed /low-power applications
CO3	Apply unfolding in the design of parallel architecture.
CO4	Evaluate the use of look-ahead techniques in parallel and pipelined IIR Digital filters.
CO5	Develop an algorithm or architecture or circuit design for DSP applications

Text Books:	
1.	Keshab K.Parthi , VLSI Digital Signal Processing systems, Design and implementation, Wiley, 1999
2.	Mohammed Isamail and Terri Fiez , Analog VLSI Signal and Information Processing, Mc Graw-Hill, 1994
3.	S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985
4.	Jose E. France, Yannis Tsividis, Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing. Prentice Hall, 1994
5.	Lars Wanhammar, DSP Integrated Circuits, Academic Press Series in Engineering,

	1st Edition

CIE Assessment:
CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests - Mini Project / Case Studies (10 Marks) - Activities/Experimentations related to courses (10 Marks)
SEE Assessment:
vii. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus. viii. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions. ix. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	-	-	-	-	2	1	1	2
CO2	3	3	3	2	-	-	-	-	2	1	1	2
CO3	3	3	3	3	-	-	-	-	2	1	1	2
CO4	3	3	3	3	-	-	-	-	2	1	1	2
CO5	3	3	2	-	3	-	-	-	3	1	3	3

High-3, Medium-2, Low-1

Course Title	**ADVANCES IN IMAGE PROCESSING**	**Semester**	III
Course Code	MVJ22LVL323	**CIE**	50
Total No. of Contact Hours	40	**SEE**	50
No. of Contact Hours/week	3 (L : T : P :: 3 : 0 : 0)	**Total**	100
Credits	3	**Exam. Duration**	3 Hours

Course objective is to:

- Understand the representation of the digital image and its properties.
- Apply pre-processing techniques required to enhance the image for its further analysis.
- Use segmentation techniques to select the region of interest in the image for analysis.
- Represent the image based on its shape and edge information and also describe the objects present in the image based on its properties and structure.
- Use morphological operations to simplify images, and quantify and preserve the main shape characteristic of the objects.

Module-1	
Image representations and properties: Image representations a few concepts, Image digitization, Digital image properties, Color images. **Video link / Additional online information :** **1. https://archive.nptel.ac.in/courses/105/107/105107160/** **2. https://nptel.ac.in/courses/108101093**	**8Hrs.**
Module-2	
Image Pre-processing: Pixel brightness transformations, geometric transformations, local pre-processing. **Laboratory Sessions/ Experimental learning:** 1. Perform different brightness transform using any tool supports image	**8Hrs.**

processing. **Video link / Additional online information:** **1. https://archive.nptel.ac.in/courses/117/105/117105135/** **2. https://www.digimat.in/nptel/courses/video/117105135/L01.html**	
Module-3	**8Hrs.**
Segmentation: Thresholding; Edge-based segmentation – Edge image thresholding, Edge relaxation, Border tracing, Hough transforms; Region – based segmentation – Region merging, Region splitting, Splitting and merging, Watershed segmentation, Region growing post-processing. **Video link / Additional online information:** **1. https://nptel.ac.in/courses/117105079** **2. https://archive.nptel.ac.in/courses/106/105/106105032/**	
Module-4	**8Hrs.**
Shape representation and description: Region identification; Contour-based shape representation and description – Chain codes, Simple geometric border representation, Fourier transforms of boundaries, Boundary description using segment sequences, B-spline representation; Region-based shape representation and description – Simple scalar region descriptors, Moments, Convex hull. **Video link / Additional online information :** **1. https://hits.digimat.in/nptel/courses/video/117105079/L37.html** **2. https://archive.nptel.ac.in/courses/109/104/109104088/**	
Module-5	**8Hrs.**
Mathematical Morphology: Basic morphological concepts, Four morphological principles, Binary dilation and erosion, Skeletons and object marking, Morphological segmentations and watersheds. **Laboratory Sessions/ Experimental learning:** 1. Image Enhancement Using Intensity Transformations 2. Morphological and Other Set Operations	

3. Two-Dimensional Fast Fourier Transform **Video link / Additional online information:** **1. https://nptel.ac.in/courses/117105079** **2. http://acl.digimat.in/nptel/courses/video/117105079/L33.html**	

Course outcomes:	
CO1	Understand the representation of the digital image and its properties.
CO2	Apply pre-processing techniques required to enhance the image for its further analysis.
CO3	Use segmentation techniques to select the region of interest in the image for analysis.
CO4	Represent the image based on its shape and edge information and also describe the objects present in the image based on its properties and structure.
CO5	Use morphological operations to simplify images, and quantify and preserve the main shape characteristics of the objects

Text Books:	
1.	Rafael C. Gonzalez and Richard E. Wood, "Digital Image Processing", Third Edition, Pearson Education
2.	S. Jayaraman, S. Esakkirajan, and T. Veerakumar. Digital Image Processing. Tata McGraw Hill, 3rd edition, 2010.

CIE Assessment:
CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests - Mini Project / Case Studies (10 Marks) - Activities/Experimentations related to courses (10 Marks)

SEE Assessment:

x. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus.

xi. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions.

xii. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	-	-	-	-	2	1	1	2
CO2	3	3	3	2	-	-	-	-	2	1	1	2
CO3	3	3	3	3	-	-	-	-	2	1	1	2
CO4	3	3	3	3	-	-	-	-	2	1	1	2
CO5	3	3	2	-	3	-	-	-	3	1	3	3

High-3, Medium-2, Low-1

Course Title	**RECONFIGURABLE COMPUTING**	**Semester**	III
Course Code	MVJ22LVL331	**CIE**	50
Total No. of Contact Hours	40	**SEE**	50
No. of Contact Hours/week	3 (L : T : P :: 3 : 0 : 0)	**Total**	100
Credits	3	**Exam. Duration**	3 Hours

Course objective is to:

- To understand the Reconfigurable vs Processor based system
- To understand the Reconfigurable Architecture
- To know Partial Reconfiguration Design
- To study Reconfigurable computing for DSP

Module-1	
Introduction: History, Reconfigurable vs Processor based system, RC Architecture. **Reconfigurable Logic Devices:** Field Programmable Gate Array, Coarse Grained Reconfigurable Arrays. Reconfigurable Computing System: Parallel Processing on Reconfigurable Computers, A survey of Reconfigurable Computing System. **Video link / Additional online information :** **1. https://nptelvideos.com/video.php?id=2396** **2. https://archive.nptel.ac.in/courses/108/105/108105118/**	**8Hrs.**
Module-2	
Languages and Compilation: Design Cycle, Languages, HDL, High Level Compilation, Low level Design flow, Debugging Reconfigurable Computing Applications. **Video link / Additional online information:** **1. https://onlinecourses.nptel.ac.in/noc21_cs96/preview**	**8Hrs.**

2. http://acl.digimat.in/nptel/courses/video/117101004/L19.html	
Module-3	**8Hrs.**
Implementation: Integration, FPGA Design flow, Logic Synthesis. **High Level Synthesis for Reconfigurable Devices:** Modelling, Temporal Partitioning Algorithms. **Video link / Additional online information:** **1. https://archive.nptel.ac.in/courses/106/106/106106088/** **2. http://acl.digimat.in/nptel/courses/video/108103108/L02.html**	
Module-4	**8Hrs.**
Partial Reconfiguration Design: Partial Reconfiguration Design, Bitstream Manipulation with JBits, The modular Design flow, The Early Access Design Flow, Creating Partially Reconfigurable Designs, Partial Reconfiguration using Hansel-C Designs, Platform Design **Video link / Additional online information :** **1. https://nptel.ac.in/courses/117106092** **2. https://archive.nptel.ac.in/courses/117/106/117106149/**	
Module-5	**8Hrs.**
Signal Processing Applications: Reconfigurable computing for DSP, DSP application building blocks, Examples: Beamforming, Software Radio, Image and video processing, Local Neighbourhood functions, Convolution. **System on a Programmable Chip:** Introduction to SoPC, Adaptive Multiprocessing on Chip **Video link / Additional online information:** **1. https://archive.nptel.ac.in/courses/108/105/108105157/** **2. https://www.digimat.in/nptel/courses/video/108105157/L15.html**	

Course outcomes:	
CO1	Understand the fundamental principles and practices in reconfigurable

	architecture.
CO2	Simulate and synthesize the reconfigurable computing architectures.
CO3	Understand the FPGA design principles, and logic synthesis
CO4	Integrate hardware and software technologies for reconfiguration computing focusing on partial reconfiguration design.
CO5	Design digital systems for a variety of applications on signal processing and system on chip configurations

Text Books:	
1.	Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays M. Gokhale and P. Graham Springer
2.	Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications C. Bobda Springer

CIE Assessment:

CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests

- Mini Project / Case Studies (10 Marks)
- Activities/Experimentations related to courses (10 Marks)

SEE Assessment:

xiii. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus.

xiv. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions.

xv. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	-	-	-	-	2	1	1	2
CO2	3	3	3	2	-	-	-	-	2	1	1	2
CO3	3	3	3	3	-	-	-	-	2	1	1	2
CO4	3	3	3	3	-	-	-	-	2	1	1	2
CO5	3	3	2	-	3	-	-	-	3	1	3	3

High-3, Medium-2, Low-1

Course Title	**LONG TERM RELIABILITY OF VLSI SYSTEMS**	**Semester**	III
Course Code	MVJ22LVL332	**CIE**	50
Total No. of Contact Hours	40	**SEE**	50
No. of Contact Hours/week	3 (L : T : P :: 3 : 0 : 0)	**Total**	100
Credits	3	**Exam. Duration**	3 Hours

Course objective is to:

- To understand Overview of Nano science and engineering.
- To learn Quantum confinement in semiconductor nanostructures.
- To analyze different fabrication process and physical process.
- To understand various types of methods of measuring properties of Nanoelectronics
- To understand various types of applications of Nanoelectronics

Module-1	
Electromigration Reliability: Why Electromigration Reliability?,Why system-level EM Reliability Management? Physics- based EM Modeling, Electromigration Fundamentals, Stress based EM Modeling and stress diffusion equations, Modeling for transient EM effects and Initial stress conditions, post voiding stress and void volume evolution, compact physics based EM model for a single wire, other relevant EM models and analysis methods. **Video link / Additional online information :** **1.** **https://www.youtube.com/watch?v=d0OVqI4naRA** **2.** **https://www.youtube.com/watch?v=i2Sc42LIiP0**	**8Hrs.**
Module-2	
Fast EM Stress Evolution Analysis: Introduction, The LTI ordinary differential equations for EM stress evolution, The presented Krylov fast EM stress analysis, Numerical results and discussions	**8Hrs.**

Video link / Additional online information: **1. http://acl.digimat.in/nptel/courses/video/108101167/L07.html** **2. https://www.youtube.com/watch?v=_sNDVdRYYbI**	
Module-3	**8Hrs.**
EM Assessment for Power Grid Networks: New power grid reliability analysis method, cross-layout temperature and thermal stress characterization, impact of across-layout temperature and thermal stress on EM. **Video link / Additional online information:** **1. http://digimat.in/nptel/courses/video/108107113/L36.html** **2. https://www.digimat.in/nptel/courses/video/117108141/L109.html**	
Module-4	**8Hrs.**
Transistor Aging Effects and Reliability: Introduction, Transistor reliability in advanced technology nodes, Transistor Aging, BTI- Bias Temperature Instability, HCI – Hot Carrier Injection, Coupling models for BTI and HCI degradations, RTN – Random Telegraph Noise, TDDB – Time Dependent Dielectric Breakdown. **Video link / Additional online information :** **1. https://www.youtube.com/watch?v=XHWww2PE7aY** **2. https://archive.nptel.ac.in/courses/115/102/115102014/**	
Module-5	**8Hrs.**
Aging Effects in Sequential Elements: Introduction, Background: flip flop timing analysis, process variation model, voltage droop model, Robustness analysis, reliability-aware flip-flop design **Video link / Additional online information:** **1. https://www.youtube.com/watch?v=Dvwq2eueNZk** **2. https://www.youtube.com/watch?v=Fy9wOF2M-oE**	

Course outcomes:	
CO1	Comprehend the recent research in the area of interconnect and device

	reliability.
CO2	Determine the impact of device-level reliability on system performance, built upon physics-based models.
CO3	Understand the physics-based EM modeling.
CO4	Understand the underlying phenomena of BTI, HCI, TDDB leading to device-level reliability degradation.
CO5	Relate to considerations at the circuit-level with both combinational and sequential elements

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Text Books:	
1.	Long-Term Reliability of Nanometer VLSI Systems Sheldon X. D. Tan, Mehdi Springer International 1st Edition, 2019 BaradaranTahoori, Publishing

CIE Assessment:
CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests - Mini Project / Case Studies (10 Marks) - Activities/Experimentations related to courses (10 Marks)
SEE Assessment:
xvi. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus. xvii. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions. xviii. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping												
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	-	-	-	-	2	1	1	2
CO2	3	3	3	2	-	-	-	-	2	1	1	2
CO3	3	3	3	3	-	-	-	-	2	1	1	2
CO4	3	3	3	3	-	-	-	-	2	1	1	2
CO5	3	3	2	-	3	-	-	-	3	1	3	3

High-3, Medium-2, Low-1

Course Title	**CMOS RF Circuit Design**	**Semester**	III
Course Code	MVJ22LVL333	**CIE**	50
Total No. of Contact Hours	40	**SEE**	50
No. of Contact Hours/week	3 (L : T : P :: 3 : 0 : 0)	**Total**	100
Credits	3	**Exam. Duration**	3 Hours

Course objective is to:

- To study State-of-the art approaches of power estimation and reduction.
- To understand power dissipation at various levels of design

Module-1	
Introduction to RF Design, Wireless Technology and Basic Concepts: A wireless world, RF design is challenging, The big picture. General considerations, Effects of Nonlinearity, Noise, Sensitivity and dynamic range, Passive impedance transformation. Scattering parameters, Analysis of nonlinear dynamic systems, conversion of gains and distortion **Video link / Additional online information :** **1.** **https://www.youtube.com/watch?v=T0Kbt7CcqUA** **2.** **https://www.youtube.com/watch?v=vtiup1w1c4E**	**8Hrs.**
Module-2	
Communication Concepts: General concepts, analog modulation, digital modulation, spectral re-growth, coherent and non-coherent detection, Mobile RF communications, Multiple access techniques, Wireless standards **Video link / Additional online information:** **1.** **https://www.youtube.com/watch?v=KUDGGsyh1Hs&list=PLbMVogVj5nJQdGDSx243YPnNeLMBrhNE8** **2.** **https://www.youtube.com/watch?v=q9k9FPh0iJI&list=PLbMVogVj5nJQdGDSx243YPnNeLMBrhNE8&index=2**	**8Hrs.**

Module-3	8Hrs.
Transceiver Architecture: General considerations, Receiver architecture, Transmitter architectures, Direct conversion and two-step transmitters, RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub-sampled receivers. **Video link / Additional online information:** 1. https://www.youtube.com/watch?v=lp5AmXEezx4&list=PLbMVogVj5nJQdGDSx243YPnNeLMBrhNE8&index=3 2. https://www.youtube.com/watch?v=Nb8NHHclch4&list=PLbMVogVj5nJQdGDSx243YPnNeLMBrhNE8&index=4	
Module-4	**8Hrs.**
Low Noise Amplifiers and Mixers: General considerations, Problem of input matching, LNAtopologies: common-source stage with inductive load, common-source stage with resistive feedback. Mixers-General considerations, passive down conversion mixers, Various mixers- working and implementation. **Video link / Additional online information :** 1. https://www.youtube.com/watch?v=kPnr_57oii4&list=PLbMVogVj5nJQdGDSx243YPnNeLMBrhNE8&index=6 2. https://www.youtube.com/watch?v=BmrnqblXoPY&list=PLbMVogVj5nJQdGDSx243YPnNeLMBrhNE8&index=12	
Module-5	**8Hrs.**
VCO and PLLs- Oscillators : Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency **Synthesizers :** PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design. **Laboratory Sessions/ Experimental learning:** 1. Image Enhancement Using Intensity Transformations, 2. Morphological and Other Set Operations	

3. Two-Dimensional Fast Fourier Transform **Video link / Additional online information:** **1. https://www.youtube.com/watch?v=BmrnqblXoPY&list=PLbMVogVj5nJQdGDSx243YPnNeLMBrhNE8&index=12** **2. https://www.youtube.com/watch?v=Hh1YraQkEXE&list=PLbMVogVj5nJQdGDSx243YPnNeLMBrhNE8&index=16**	

Course outcomes:	
CO1	Identify the sources of power dissipation in CMOS circuits.
CO2	Perform power analysis using simulation-based approaches and probabilistic analysis.
CO3	Use optimization and trade-off techniques that involve power dissipation of digital circuits.
CO4	Make the power design a reality by making power dimension an integral part of the design process.
CO5	Use practical low power design techniques and their analysis at various levels of design abstraction and analyse how these are being captured in the latest design automation environments.

Text Books:	
1.	RF Microelectronics B. Razavi PHI second edition
2.	CMOS Circuit Design, layout and Simulation R. Jacob Baker, H.W. Li, D.E. Boyce PHI 1998

CIE Assessment:
CIE is based on quizzes, tests, assignments/seminars and any other form of evaluation. Generally, there will be: Three Internal Assessment (IA) tests during the semester (30 marks each), the final IA marks to be awarded will be the average of three tests

- Mini Project / Case Studies (10 Marks)
- Activities/Experimentations related to courses (10 Marks)

SEE Assessment:

xix. Question paper for the SEE consists two parts i.e. Part A and Part B. Part A is compulsory and consists of objective type or short answer type questions of 1 or 2 marks each for total of 20 marks covering the whole syllabus.

xx. Part B also covers the entire syllabus consisting of five questions having choices and may contain sub-divisions, each carrying 16 marks. Students have to answer five full questions.

xxi. One question must be set from each unit. The duration of examination is 3 hours.

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	-	-	-	-	2	1	1	2
CO2	3	3	3	2	-	-	-	-	2	1	1	2
CO3	3	3	3	3	-	-	-	-	2	1	1	2
CO4	3	3	3	3	-	-	-	-	2	1	1	2
CO5	3	3	2	-	3	-	-	-	3	1	3	3

High-3, Medium-2, Low-1