MVJ College of Engineering, Whitefield, Bangalore 560067

An Autonomous Institution, Affiliated to VTU, Belagavi

M.Tech in Electronics and Communication (VLSI Design and Technology)

Scheme of Teaching and Examination

Outcome Based Education (OBE) and Choice Based Credit System (CBCS)

Effective from the Academic Year 2024-25

I SEMESTER

Sl. No.	Course Type	Course Code	Course Title	Teaching Hours perWeek			Examination				Credits
				Theory	Practical/ Seminar	Tutorial/SDA	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	P	T/SDA					
1	PCC	MVJLVD11	MOS Device Physics	3	0	0	03	50	50	100	3
2	IPCC	MVJLVD12	Analog Integrated Circuit Design	3	2	0	03	50	50	100	4
3	PCC	MVJLVD13	Digital System Design using FPGA	3	0	0	03	50	50	100	3
4	PEC	MVJLVD14X	Professional Elective I	3	0	0	03	50	50	100	3
5	PEC	MVJLVD15X	Professional Elective II	3	0	0	03	50	50	100	3
6	PECL	MVJLVDL16X	FPGA based Digital Circuit Design	0	4	0	03	50	50	100	2
7	NCMC	MVJRMI17	Research Methodology and IPR (Online)	Online Courses (online.vtu.ac.in)							PP
								300	**300**	**600**	**18**

Professional Elective I		**Professional Elective II**	
MVJLVD141	ASIC Design	MVJLVD151	Memory Technologies
MVJLVD142	VLSI Testing	MVJLVD152	Advanced Embedded Systems
MVJLVD143	Optoelectronics material and Devices	MVJLVD153	VLSI Interconnects
MVJLVD144	Biosensors and Circuits	MVJLVD154	VLSI Architectures for AI
Lab			
MVJLVDL161	FPGA based Digital Circuit Design		

Note: **7oi** Science Courses, **PCC**: Professional core. **IPCC**- Integrated Professional Core Courses, **PCC(PB):** Professional Core Courses (Project Based), **PCCL**-Professional Core Course lab, **NCMC**- None Credit Mandatory Course, **L-**Lecture**, P-**Practical**, T/SDA-**Tutorial / Skill Development Activities (Hours are for Interaction between faculty and students) **MRMI107** - Research Methodology and IPR (**Online**) for the students who have **not studied** this course in the Undergraduate level. This course is not counted for vertical progression, Students have to qualify for the award of the master's degree.

M- Master program **xx** – **ME** for Mechanical Engineering Stream, **CV** for Civil Engineering Stream, **EE** – Electrical & Electronics Engineering Stream, **EC-** Electronics and Communication Engineering Stream, **CS**- Computer Science and Engineering, **BA**-
Business Administration **AR**- Architecture- etc.

BSC: Basic Science Courses: Courses like Mathematics/ Science are the prerequisite courses that the concerned engineering stream board of Studies will decide.
PCC: Professional Core Course: Courses related to the stream of engineering, which will have both CIE and SEE components, students have to qualify in the course for the award of the degree.

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Integrated Professional Core Course (IPCC): Refers to a Professional Theory Core Course Integrated with practical's of the same course. The IPCC's theory part shall be evaluated by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. **Project Based Learning Course (PCC(PB):** Project Based Learning course is a professional core Course only Students have to complete a project out of learning from the course and SEE will be viva voce on project work. **PCCL: Professional Core Course Laboratory:** Practical courses whose CIE will be evaluated by the class teacher and SEE will be evaluated by the two examiners.

Skill development activities: Under Skill development activities in a concerning course, the students should

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in the modelling of systems and algorithms for transient and SteadyState operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s are to be involved either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities that will enhance their skills. The prepared report shall be evaluated for CIE marks.

MRMI107 - Research Methodology and IPR- None Credit Mandatory Course (NCMC) if students have not studied this course in their undergraduate program then he /she has to take this course at **http://online.vtu.ac.in** and to qualify for this course is compulsory before completion of the minimum duration of the program (Two years), however, this course will not be considered for vertical progression.

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Effective from the Academic Year 2024-25

Semester- I

MOS DEVICE PHYSICS			
Course Code	**MVJLVD11**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- To introduce the energy band diagrams, electrostatics, and operational modes of MOS capacitors
- To explore nonidealities in MOS structures along with the physics and reliability issues of MOSFET devices
- To analyze the working principles, electrostatics, and unique characteristics of SOI MOSFETs
- To examine nanoscale transistor technologies, focusing on diffusive, quasi-ballistic, and ballistic transport mechanisms in planar and nanowire FETs using both classical and quantum approaches.
- To study advanced MOSFET architectures, highlighting their role in improving transistor performance at nanoscale dimensions

Module-1

MOS Capacitor: Energy band diagram of Metal-Oxide-Semiconductor contacts, Mode of Operations: Accumulation, Depletion, Midgap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation, CV characteristics of MOS, LFCV and HFCV.

RBT Levels: L2, L3

Module-2

Nonidealities in MOS, oxide fixed charges, interfacial charges, Midgap gate Electrode, Poly-Silicon contact, Electrostatics of non-uniform substrate doping, ultrathin gate-oxide and inversion layer quantization, quantum capacitance, MOS parameter extraction.

Physics of MOSFET: Drift-Diffusion Approach for IV, Gradual Channel Approximation, Sub-threshold current and slope, Body effect, Pao & Sah Model, Detail 2D effects in MOSFET, High field and doping dependent mobility
models, High field effects and MOSFET reliability issues (SILC, TDDB, & NBTI)

RBT Levels: L3

Module-3

SOI MOSFET: FDSOI and PDSOI, 1D Electrostatics of FDSOI MOS, VT definitions, Back gate coupling and body effect parameter, IV characteristics of FDSOI-FET, FDSOI-sub-threshold slope, Floating body effect, single transistor latch, ZRAM device, Bulk and SOI FET: discussions referring to the ITRS

RBT Levels: L3

Module-4

Nanoscale Transistors: Diffusive, Quasi Ballistic & Ballistic Transports, Ballistic planer and nanowire-FET modeling: semi-classical and quantum treatments**.**

RBT Levels: L3

Module-5

Advanced MOSFETs: Strain Engineered Channel materials, Mobility in Strained materials, Electronics of double gate and Fin-FET devices.

RBT Levels: L3, L4

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements (passed) and earned the credits allotted to each subject/ course if the student secures not less than 50% of the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of 50 Marks.
2. Two assignments each of 20 Marks or one Skill Development Activity of 40 marks to attain the COs and POs.

The sum of three tests, two assignments/skill Development Activities, will be scaled down to 50 marks. CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four subquestions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module.

Suggested Learning Resources:

Books

Textbooks

1. S.M. Sze & Kwok K. Ng, Physics of Semiconductor Devices, Wiley S.M. Sze & Kwok K. Ng, Physics of Semiconductor Devices, Wiley.
2. Yuan Taur & Tak H. Ning, Fundamentals of Modern VLSI Devices, Cambridge.

Reference Books

1. Mark Lundstrom & Jing Guo, Nanoscale Transistors: Device Physics, Modeling & Simulation, Springer.

Web links and Video Lectures (e-Resources):

- https://www.youtube.com/watch?v=h0Y9jDKqScQ
- https://www.youtube.com/watch?v=WiIdfUWjXog

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Analyze the energy band diagrams, electrostatics, and operational modes of MOS capacitors	L3
CO2	Evaluate the impact of nonidealities in MOS structures, while extracting MOS parameters.	L4
CO3	Explain the working principles and characteristics of SOI MOSFETs	L2

Sl. No.	Description	Blooms Level
CO4	Examine nanoscale transistor models with diffusive, quasi-ballistic, and ballistic transport mechanisms using both classical and quantum approaches.	L2
CO5	Analyze advanced MOSFET architectures for improved performance in nanoscale technologies	L4

Semester- I

ANALOG INTEGRATED CIRCUIT DESIGN			
Course Code	**MVJLVD12**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:2:0	SEE Marks	50
Total Hours of Pedagogy	40theory+ 10-12lab hours	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- To understand and analyze the small signal models for MOS transistors, and design various analog CMOS sub-circuits
- To design and implement CMOS operational amplifiers (op-amps) using various topologies
- To develop high-performance CMOS operational amplifiers with characteristics such as buffered op-amps, high-speed op-amps, low-noise op-amps, and low-voltage op-amps
- To analyze and design switched capacitor circuits, and model their behavior in the Z-domain for various orders of filters
- To understand and design digital-to-analog (DAC) and analog-to-digital (ADC) converters

Module-1

ANALOG CMOS SUB-CIRCUITS: Small Signal Model For MOS, MOS Switch, MOS Resistors, Current Sink/Source, High Input Impedance Current Mirrors, Differential, Cascode and Current Amplifiers, Output Amplifiers, High Gain Amplifier Architectures

RBT Levels: L2, L3

Module-2

CMOS OPERATIONAL AMPLIFIERS: Design of CMOS Operational Amplifiers, Telescopic Op-amp topologies, Compensation, Design of Two Stage Op-Amps, Cascode Op-Amps, Simulation and Measurement Techniques

RBT Levels: L3

Module-3

HIGH PERFORMACE CMOS OP-AMPS: Buffered Op-Amps, High Speed/Frequency Op-Amps, Differential Output Op-Amps, Micro Power Op- Amps, Low Noise and Low Voltage Op-Amps.

RBT Levels: L3

Module-4

SWITCHED CAPACITOR FILTERS: Switched Capacitor Circuits: Design and Analysis, Switched Capacitor Amplifiers, Switch Capacitor Integrators, Z Domain Models, 1st And 2nd Order Switch Capacitor Filters, Higher Order Filters.

RBT Levels: L3

Module-5

D/A AND A/D CONVERTERS

Sample And Hold Circuits. Characterization of DAC, Nyquist Rate, Parallel DAC, Extending Resolution of Parallel DAC, Serial DAC, Characterization Of ADC, Serial ADC, High Speed ADC, Over Sampling Techniques.

RBT Levels: L3, L4

PRACTICAL COMPONENT OF IPCC

1.	Draw the CMOS schematic and Layout of the inverter circuit, simulate both schematic and layout to determine propagation delay, rise time and Q point and comment on the results.
2.	Design the common source amplifier schematic for a gain of 30dB and also draw the layout of the scheme, simulate the layout for ac analysis and comment the results.

3.	Design the common Drain amplifier schematic and also draw the layout of the same, simulate the layout for ac analysis and comment on results.
4.	Design the common Gate amplifier schematic (Current Gain of 30 dB) and also draw the layout of the same, simulate the layout for ac analysis and comment on results.
5.	Design the Differential amplifier schematic for a gain of 50dB.
6.	Design the op-amp schematic with using differential and also draw the layout of the same, simulate the layout for ac analysis and comment on results.
7.	Design the schematic of current mirror, simulate and do ac analysis and comment on results.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

Suggested Learning Resources:

Text Book:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

'**Reference Books:**

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.

Web links and Video Lectures (e-Resources):

https://www.youtube.com/playlist?list=PLbMVogVj5nJRlMz5diOg9wBizaU6-egJc
http://www.digimat.in/nptel/courses/video/117108038/L01.html

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No	Description	Blooms Level
CO1	Analyze and model small-signal behavior of MOS transistors and design basic analog CMOS sub-circuits.	L3,L4
CO2	Design CMOS operational amplifiers using various topologies and apply compensation techniques and simulation methods to optimize the performance of op-amps.	L3,L4
CO3	Design and implement high-performance CMOS op-amps with characteristics such as high-speed, low-noise, and low-voltage operation, addressing specific requirements for different applications.	L4
CO4	Design and analyze switched-capacitor circuits, including amplifiers, integrators, and filters, and effectively model these circuits in the Z-domain for higher-order	L4

		filters.	
	CO5	Design digital-to-analog (DAC) and analog-to-digital (ADC) converters, implement sample-and-hold circuits, and characterize the performance of high-speed ADCs using oversampling techniques	L4

Semester- I

DIGITAL SYSTEM DESIGN USING FPGA			
Course Code	**MVJLVD13**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory	Total Marks	100
Credits	04	Exam Hours	03

Course Learning Objectives: This course will enable students:

- Understand design methodology and flow of FPGA and ASIC design style
- Apply FPGA implementation for combinational logic circuits
- Apply FPGA implementation for sequential logic circuits
- Understand and implement storage and PLA devices
- Understand IP based system design and its real time validation cum debug

Module - 1

Prerequisites: Digital Circuits Design

Introduction to Digital Design Methodology: Brief introductions of Design Specification, Design Partition, Design Entry, Simulation and Functional Verification, Design Integration and Verification, Pre-synthesis Sign-Off, Gate-Level Synthesis and Technology Mapping, Post-synthesis Design Validation, Post synthesis, Timing Verification, Test Generation and Fault Simulation, Placement and Routing, Physical and Electrical Design Rule Checks, Parasitic Extraction, Design Sign-Off.

Brief introduction of FPGA and ASIC, Design Flows: FPGA vs ASIC (Book: Advances in Digital Design by M clitti)

Basics of Verilog-HDL: Introduction, Structural, Data-flow and Behavioural with data-types and procedural behaviour (Self-Study for programming the FPGA)

RBT Levels: L2, L3

Module – 2

Review of Combinational Logic Design:

Combinational Logic and Boolean Algebra: Boolean Algebra, De-Morgan's Laws, Theorems for Boolean Algebraic Minimization.

Representation of Combinational Logic: Sum-of-Product Representation, Product-of-Sums Representation, Simplification of Boolean Expressions: Karnaugh Maps (SOP, POS), Glitches and Hazard,

Building Blocks for Logic Design: NAND-NOR Structures, Multiplexers, De-multiplexers, Encoders, Decoder.

Module – 3

Review of Sequential Logic Design:

Storage Elements: Latches, Transparent Latches, Flip-Flops: S-R-FF, D-FF, JK, Master-Slave JK, T-FF, Register, counter, Design of Sequential Machines: Finite State Machine, Sequence detector, Design Example: BCD to Excess-3 Code Converter, 1011 Sequence detector using melay and moore machine.

Module – 4

Programmable Logic and Storage Devices:

Storage Devices: Read-Only Memory (ROM), PROM, EPROM, EEPROM, RAM- Static and dynamic RAM, RAM: Static and dynamic RAM: Architecture, READ-WRITE operation and Comparisons,

Programmable Logic Devices: Programmable Logic Array (PLA), Programmable Array Logic (PAL)

Module – 5

Programmable Logic Devices: Complex PLDs (CPLDs), Field Programmable Gate Arrays (FPGA): Architecture of FPGA, Role of FPGA in ASIC markets

Embeddable and Programmable IP Cores for a System-on-a-Chip (SoC), Basics of AXI interfacing (Master-Slave), IP-based counter implementation, IP-based different clock generator, FIFO

Real Time Logic Validations: Virtual input and output (VIO), and Integrated logic Analyzer (Xilinx ILA IP).

Suggested Learning Resources:

Textbooks:

1. Michael D Ciletti —Advances in Digital Design with Verilog, Prentice Hall of India, Second Edition, 2017
2. Palnitkar, S. "Verilog HDL: A guide to Digital Design and Synthesis" 2nd ed. Pearson.
3. Sass, Ronald, and Andrew G. Schmidt, "Embedded systems design with platform FPGAs: Principles and practices", Morgan Kaufmann.

Reference Books:

1. Charles H Roth Jr., Larry L. Kinney —Fundamentals of Logic Design, Cengage Learning 7th Edition.
2. Donald D. Givone, "Digital Principles and Design", McGraw Hill.

Web links and Video Lectures (e-Resources):

https://archive.nptel.ac.in/courses/117/108/117108040/
https://onlinecourses.nptel.ac.in/noc23_ee29/preview

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No	Course Outcomes	Blooms Level
CO 1	Explain the stages of digital design methodology and differentiate between FPGA and ASIC design flows.	L2
CO 2	To understand combinational logic circuits and implementation on FPGA platform	L2
CO 3	Able to design and implement sequential circuits on FPGA platform	L4
CO 4	Able to understand and implement the storage device on FPGA platform	L2
CO 5	Implement IP-based designs and validate using tools like Virtual Input/Output (VIO) and Integrated Logic Analyzer (ILA).	L4

Semester- I

FPGA BASED DIGITAL CIRCUIT DESIGN			
Course Code	**MVJLVDL16X**	CIE Marks	50
Teaching Hours/Week (L:P:T/SDA)	0:2:0	SEE Marks	50
Credits	02	Exam Hours	03

Course Objectives: This course will enable students to:

- Understand the combination logic implementation on FPGA
- Understand the Sequential logic implementation on FPGA
- Apply logic to generate different clock signals as per specifications
- Understand IP based logic implementation on FPGA
- Apply and validate real time of digital logic on FPGA platform

PART A

Sl.No.	Experiments
1	Write Verilog program for Logic gates (AND, NOT, OR, XOR) combinational logic, verify the design using test bench and perform the synthesis by downloading the design on to FPGA device.
2	Write Verilog program for Full adder and Substractor combinational logic, verify the design using test bench and perform the synthesis by downloading the design on to FPGA device.
3	Write Verilog program for Sequential Circuits of FFs (D, J-K and T), verify the design using test bench and perform the synthesis by downloading the design on to
4	Structural modeling of b. BCD to Excess-3 code converter
5	Write Verilog program for the following Sequential Circuits, verify the design using test bench and perform the synthesis by downloading the design on to FPGA device. SISO and PISO shift register b. 4-Bit Linear Feedback shift register
6	Write Verilog program for Ring Counter verify the functionality using test bench and perform the synthesis by downloading the design on to FPGA device.

PART B

7	Write a Verilog code to design a clock divider circuit that generates 1/2, 1/3rdand 1/4thclock from a given input clock. Port the design to FPGA and validate the Functionality through ILA.
8	Generate 3 different clock frequencies using predefined IP and validate using oscilloscopes.
9	Write a Verilog code to interface LED and display HDL on the LED display and also validate all output using VIO IP before implementations
10	Design an FSM to detect 1010 patterns and validate real time detection of patterns using ILA IP

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 40% of maximum marks in the semester-end examination (SEE). In total of CIE and SEE student has to secure 50% maximum marks of the course.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- **Total marks scored by the students are scaled down to 30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 01 tests for 100 marks, test shall be conducted after the 14th week of the semester.
- In test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- **The test marks are scaled down to 20 marks** (40% of the maximum marks).

The Sum of **scaled-down** marks scored in the report write-up/journal and marks of test is the total CIEmarks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute; examiners are appointed by the University.

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 10% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Semester- I

ASIC DESIGN			
Course Code	**MVJLVD141**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- Understand the fundamental concepts and design flow of ASICs
- Analyze various programmable ASIC technologies
- Examine the design and synthesis of programmable ASIC logic cells
- Implement ASIC floor planning, placement, and routing techniques by studying physical design flow
- Apply optimization algorithms in ASIC design to solve routing challenges

Module-1

INTRODUCTION TO ASIC'S: Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell - Sequential logic cell - Data path logic cell - Transistors as Resistors – Transistor Parasitic Capacitance- Logical effort -Library cell design - Library architecture.

RBT Levels: L2, L3

Module-2

PROGRAMMABLE ASIC'S: Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT -Xilinx LCA -Altera FLEX - Altera MAX DC and AC inputs and outputs - Clock and Power inputs - Xilinx I/O blocks.

RBT Levels: L3

Module-3

PROGRAMMABLE ASIC LOGIC CELLS: Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX -Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

RBT Levels: L3

Module-4

ASIC FLOOR PLANNING, PLACEMENT AND ROUTING: ASIC Construction: Physical Design- System Partitioning- FPGA Partitioning- Partitioning Methods. Floor planning and Placement: Floor planning- Placement- Physical Design Flow. Routing: Global Routing – Detailed Routing- Special Routing.

RBT Levels: L3

Module-5

OPTIMIZATION ALGORITHMS: Planar subset problem (PSP) -single layer global routing single layer detailed routing wire length and bend minimization technique-over the cell (OTC) Routing-multichip modules (MCM)-Programmable logic arrays-Transistor chaining-Weinberger Arrays-Gate Matrix Layout-1D compaction-2D compaction.

RBT Levels: L3, L4

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements (passed) and earned the credits allotted to each subject/ course if the student secures not less than 50% of the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of 50 Marks.
2. Two assignments each of 20 Marks or one Skill Development Activity of 40 marks to attain the COs and POs.

The sum of three tests, two assignments/skill Development Activities, will be scaled down to 50 marks. CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four subquestions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

The students will have to answer five full questions, selecting one full question from each module.

Suggested Learning Resources:

Text Books

1. Michael John Sebastian Smith, "Application - Specific Integrated Circuits", Addison- Wesley Professional, 2005.
2. Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective" Addison Wesley/ Pearson education 3rdedition, 2011

Reference Books

1. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations" Springer, ISBN: 978-1-4614-1119-2. 2011.
2. Rakesh Chadha, Bhasker J, "An ASIC Low Power Primer", Springer, ISBN: 978-14614-4270-7.

Web links and Video Lectures (e-Resources):

https://www.youtube.com/watch?v=oZSv68esbgI

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Explain the design flow and types of ASICs, apply CMOS design rules, and analyze logic cells, parasitic effects, and logical effort in library cell design	L2
CO2	Compare and evaluate programmable ASIC technologies, including SRAM, Anti-fuse, EPROM, and EEPROM, and analyze the input/output characteristics of Xilinx, Altera, and Actel devices	L4

CO3	Demonstrate the ability to design and synthesize programmable ASIC logic cells using schematic entry, low-level design languages, and design tools for various ASIC families	L3
CO4	Analyze and implement floor planning, partitioning, placement, and routing techniques in ASIC design to optimize physical design flow	L4
CO5	Apply optimization algorithms to solve routing challenges, minimize wire length and bends, and implement advanced layout techniques such as transistor chaining and compaction.	L5

VLSI TESTING			
Course Code	**MVJLVD142**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course Learning objectives: This Course will enable students to

- Understand the fundamentals of Design for Testability (DFT) by analyzing testability concepts
- Explain fault simulation techniques by exploring simulation models, logic simulation, and fault simulation approaches for identifying faults in digital circuits
- Analyze and apply test generation methods such as exhaustive testing, Boolean difference, and ATPG algorithms to detect stuck-at and non-stuck-at faults in digital systems
- Understand and implement Built-In-Self-Test (BIST) by studying BIST design rules, test pattern generation, output response analysis, and various logic BIST architectures.
- Explore test compression and memory testing techniques by applying stimulus and response compression methods, analyzing RAM fault models, and generating RAM test patterns for efficient testing

Module-1

Design for Testability: Introduction, Testability Analysis, DFT Basics, Scan cell design, Scan Architecture, Scan design rules, Scan design flow

.

RBT Levels: L2

Module-2

Fault Simulation: Introduction, Simulation models, Logic simulation, Fault simulation

RBT Levels: L2, L3

Module-3

Test Generation: Introduction, Exhaustive testing, Boolean difference, Basic ATPG algorithms, ATPG for non-stuck-at faults, other issues in test generation.

RBT Levels: L2, L3

Module-4

Built-In-Self-Test: Introduction, BIST design rules, Test pattern generation, Output response analysis, Logic BIST architectures.

RBT Levels: L2, L3

Module-5

Test Compression: Introduction, Stimulus compression, Response compression.

Memory Testing: Introduction, RAM fault models, RAM test generation

RBT Levels: L3, L4

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements (passed) and earned the credits allotted to each subject/ course if the student secures not less than 50% of the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of 50 Marks.
2. Two assignments each of 20 Marks or one Skill Development Activity of 40 marks to attain the COs and POs.

The sum of three tests, two assignments/skill Development Activities, will be scaled down to 50 marks. CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module.

Suggested Learning Resources:

Text Books:

1. S. Yu, "Semiconductor Memory Devices and Circuits", 1st Edition, CRC Press, 2022.
2. Ashok K. Sharma, "Semiconductor Memories: Technology, Testing, and Reliability", 1st Edition, Wiley IEEE, 2013.
3. Kiyoo Itoh, "VLSI Memory Chip Design", 1st Edition, Springer, 2001.

Reference books:

1. N. Weste and D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 3rd Edition. Pearson, 2006.
2. Y. Nishi and Magyari-Kope, "Advances in non-volatile memory and storage technology", Woodhead Publishing, 1st Edition, 2019.

Web links and Video Lectures (e-Resources):

- https://onlinecourses.nptel.ac.in/noc20_ee76/preview
- https://archive.nptel.ac.in/courses/106/103/106103116/

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Describe the fundamentals of testability, analyze DFT concepts, and implement scan cell design, scan architectures, and design flows for improving testability.	L2
CO2	Explain fault simulation techniques and apply logic and fault simulation models to identify and analyze faults in digital circuits.	L2
CO3	Apply test generation techniques to detect stuck-at and non-stuck-at faults in digital systems	L3
CO4	Design and implement Built-In-Self-Test (BIST) systems using test pattern generation.	L4
CO5	Analyze and apply test compression methods and memory testing techniques, including stimulus/response compression and RAM fault models, to optimize testing processes	L4

OPTOELECTRONICS MATERIAL AND DEVICES			
Course Code	**MVJLVD143**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course Learning objectives: This Course will enable students to

- Understand the pre-quantum mechanics picture and the role of lattice structures
- Analyze the electrical properties of materials such as metals and semiconductors by studying their band structures, types of semiconductors, dopant levels, and mobility measurements.
- Explain the dielectric properties of materials including dielectric constants, polarization, capacitors, and insulators, and analyze electronic structures at material interfaces
- Explore the optical properties of materials through bandgap engineering, light-material interactions, carrier generation/recombination processes, and carrier transport mechanisms
- Analyze and design basic electronic devices such as p-n junctions, MOS devices, and transistors, and explore applications in solar cells, LEDs, and emerging organic electronics

Module-1

Pre-quantum mechanics picture: Drudes Model. Review of quantum mechanics and free electron theory, failures of free electron theory and introduction to the role of lattice. Review of reciprocal lattice, Brillouin zone, free electron band diagram, potential in a crystal, electron dynamics and concept of holes, conductivity in relation to band structure.

RBT Levels: L2

Module-2

Electrical Properties of Materials: Band structure of metals and semiconductors, empirical estimates of conductivity in metals and alloys. Semiconductors - band diagrams, direct and indirect bandgap, degenerate and nondegenerate semiconductors, intrinsic and extrinsic semiconductors, determination of dopant levels and mobility measurements.

RBT Levels: L2, L3

Module-3

Dielectric materials: dielectric constants and polarization, linear dielectric materials, capacitors and insulators, C-V characterization.
Electronic structure of interfaces: metal semiconductor, insulator-semiconductor, semiconductor heterostructures.

RBT Levels: L2, L3

Module-4

Optical materials: electron-hole recombination, bandgap engineering. Light interaction with materials-transparency, translucency and opacity, refraction and refractive index, reflection, absorption and transmission. Carrier generation processes, recombination processes, R-G statistics, surface R-G processes. Carrier transport, drift, diffusion, equation of state.

RBT Levels: L2, L3

Module-5

Basic Electronic Devices p-n junction their application in solar cells and light emitting diodes. MOS devices and Transistors.
Organic electronics: Thin Film Transistors, Light Emitting Diodes, Solar cells

RBT Levels: L3, L4

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements (passed) and earned the credits allotted to each subject/ course if the student secures not less than 50% of the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of 50 Marks.
2. Two assignments each of 20 Marks or one Skill Development Activity of 40 marks to attain the COs and POs.

The sum of three tests, two assignments/skill Development Activities, will be scaled down to 50 marks. CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four subquestions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module.

Suggested Learning Resources:

Textbooks:

1. Electronic Properties of Materials: An Introduction for Engineers, Rolf E. Hummel, Springer Verlag, 1985
2. Physical Properties of Semiconductors, Charles M. Wolfe, Nick Holonyak and Gregory E. Stillman, Prentice Hall, 1989.
3.

Reference Books:

1. Advanced Semiconductor Fundamentals, Robert F. Pierret as part of Modular Series on Solid State Devices Vol. 6, Addison Wesley, 1989
2. Introduction to Solid State Physics, Charles Kittel, John Wiley & Sons 1991

Web links and Video Lectures (e-Resources):

- https://archive.nptel.ac.in/courses/113/104/113104012/
- https://onlinecourses.nptel.ac.in/noc24_mm10/preview

Skill Development Activities Suggested

- The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Explain the limitations of free electron theory and analyze the role of lattice structures, reciprocal lattice, Brillouin zones, and electron dynamics in understanding material conductivity.	L2
CO2	Analyze the electrical properties of metals and semiconductors	L2, L3

CO3	Describe the dielectric properties of materials, including polarization, dielectric constants, and C-V characterization	L2, L3
CO4	Evaluate the optical properties of materials by understanding bandgap engineering	L4
CO5	Design and analyze basic electronic devices like p-n junctions, MOS devices, and transistors, and explore their applications in solar cells, LEDs, and organic electronics	L4

BIOSENSORS AND CIRCUITS			
Course Code	**MVJLVD144**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- Understand the principles of transducers and biochemical transducers
- Analyze the design and applications of bio-potential electrodes
- Examine the working principles of different electrodes for biomedical applications
- Explore the principles and operation of optical sensors and radiation detectors
- Study the working principles of biological and smart sensors

Module-1

Transducers Principles, Biochemical Transducers: Electrode theory, electrode impedance, metal electrolyte interface and electrode-tissue interface

RBT Levels: L3

Module-2

Bio-potential electrodes: micro electrodes, body surface electrodes, needle electrodes, electrodes for ECG, EEG, and EMG.

RBT Levels: L3

Module-3

Electrodes: hydrogen electrodes, Ag/AgCl electrodes, Calomel electrodes, specific ion electrodes, pH electrode, O2 and CO2 electrode.

RBT Levels: L3, L4

Module-4

Optical Sensor and Radiation Detectors: Principles of optical sensors and types of optical sensors, Optical fibers, LASERs.
Radiation detectors: Proportional counter, Gas-ionization chamber, Geiger counters, Scintillation detectors.

RBT Levels: L3

Module-5

Biological Sensors: Receptors in the human body, Ion exchange membrane electrodes, enzymatic biosensors, Basic principles of MOSFET biosensors & BIOMEMS, basic idea about Smart sensors, Biomedical Measurement.

RBT Levels: L3

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements (passed) and earned the credits allotted to each subject/ course if the student secures not less than 50% of the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of 50 Marks.
2. Two assignments each of 20 Marks or one Skill Development Activity of 40 marks to attain the COs and POs.

The sum of three tests, two assignments/skill Development Activities, will be scaled down to 50 marks. CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four subquestions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module.

Suggested Learning Resources:

Text Books

1. Josheph J. Carr and John M. Brown, —Introduction to Biomedical Equipment Technology||, 4th Edition, Pearson Education, 2001.
2. John. G. Webster, —Medical Instrumentation- Application and Design||, 4th Edition, John Wiley & Sons, 2010.

Reference Books

1. Suresh R. Devashahayan, —Signals and Systems in Biomedical Engineering||, Revised 2nd Edition, Kluwer academics/ Plenum publication, 2013.

Web links and Video Lectures (e-Resources):

- https://onlinecourses.nptel.ac.in/noc22_ph01/preview
- https://onlinecourses.nptel.ac.in/noc24_ee83/preview

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Explain the principles of transducers and biochemical transducers by analyzing electrode theory, electrode impedance, and the interaction at metal-electrolyte and electrode-tissue interfaces.	L2
CO2	Analyze the structure, working, and applications of bio-potential electrodes	L3
CO3	Evaluate the working principles and characteristics of electrodes for biomedical applications	L4
CO4	Describe the principles of optical sensors and radiation detectors	L2
CO5	Explain the working and applications of biological sensors	L2

MEMORY TECHNOLOGIES			
Course Code	**MVJLVD151**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning Objectives:

- Understand the principles and architectures of SRAM technologies
- Explore the design and operation of DRAM technologies
- Analyze non-volatile memory technologies, such as Masked ROMs, PROMs, EPROMs, EEPROMs, Flash memories, and their design principles and applications
- Examine advanced memory technologies, with an emphasis on emerging materials and devices
- Understand hybrid memory systems and reliability considerations, including 2D and 3D memory stacks, memory cards, testing methods, and issues related to memory reliability and high-density packaging

Module - 1

Random Access Memory Technologies: Static Random-access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

RBT Levels: L2, L3

Module - 2

DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs.

RBT Levels: L3

Module - 3

Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

RBT Levels: L3

Module - 4

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random-access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random-access Memories (MRAMs).

RBT Levels: L3

Module - 5

Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging.

RBT Levels: L3, L4

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements

(passed) and earned the credits allotted to each subject/ course if the student secures not less than 50% of the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of 50 Marks.
2. Two assignments each of 20 Marks or one Skill Development Activity of 40 marks to attain the COs and POs.

The sum of three tests, two assignments/skill Development Activities, will be scaled down to 50 marks. CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module.

Suggested Learning Resources:

Text Books

1. Ashok K. Sharma, "Semiconductor Memories: Technology, Testing, and Reliability", 1st Edition, Wiley IEEE, 2013
2. Ashok K. Sharma, " Semiconductor Memories Technology, Testing and Reliability "Prentice-Hall of India Private Limited, New Delhi, 1997

Reference Books

1. Wen C. Lin, "Handbook of Digital System Design", CRC Press.

Web links and Video Lectures (e-Resources):

- https://onlinecourses.nptel.ac.in/noc24_hs183/preview
- **https://www.youtube.com/playlist?list=PL1p7mdw-Ee7kfbAOjLE--cFV1HnWDIE0J**

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No	Course Outcomes	Blooms Level
CO1	Explain the principles, architectures, and cell structures of SRAM technologies	L2
CO2	Analyze the design and operation of DRAM technologies	L4
CO3	Evaluate the working principles of non-volatile memory technologies	L4
CO4	Describe advanced memory technologies, including FRAMs, MRAMs, GaAs FRAMs, and analog memories, and analyze their role in high-density memory applications	L2

CO5	Assess memory hybrid systems, including 2D and 3D memory stacks, memory cards, and memory testing techniques, and evaluate reliability issues in high-density memory packaging.	L4

ADVANCED EMBEDDED SYSTEMS			
Course Code	**MVJLVD152**	CIE Marks	50
Teaching Hours/Week(L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course Learning objectives:

- To understand the difference between Embedded Systems and General Computing Systems
- To understand the Classification of Embedded Systems based on Performance, Complexity along with the Domains and Areas of Applications of Embedded Systems
- Analysis of a RealLife example on the bonding of Embedded Technology with Human Life
- To understand the difference between Microcontrollers and ARM Cortex processors.
- To learn Programming using assembly and C language, CMSIS for variety of End Applications

Module-1

Embedded System: Embedded v/s General Computing System, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Optocoupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems.

RBT Levels: L2, L3

Module-2

Hardware Software Co-Design: Embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment(IDE),Files generated during compilation, simulators, emulators and debugging.

RBT Levels: L3

Module-3

ARM - 32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence.

RBT Levels: L3

Module-4

Instruction Sets: Assembly basics, Instruction list and description, useful instructions,Memory Systems, Memory maps, Cortex M3 implementation overview, pipeline and bus interface, Exceptions, Nested Vector interrupt controller design, Systick Timer, Cortex- M3 Programming using assembly and C language, CMSIS.

RBT Levels: L3

Module-5

Introduction to RISC - V: Operations of the Computer Hardware, Operands of the Computer Hardware, Signed and Unsigned Numbers, Representing Instructions in the Computer, Logical Operations, Instructions for Making Decisions, RISC-V Addressing for Wide Immediate and Addresses, Parallelism and Instructions: Synchronization

RBT Levels: L3, L4

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements (passed) and earned the credits allotted to each subject/ course if the student secures not less than 50% of the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of 50 Marks.
2. Two assignments each of 20 Marks or one Skill Development Activity of 40 marks to attain the COs and POs.

The sum of three tests, two assignments/skill Development Activities, will be scaled down to 50 marks. CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module.

Suggested Learning Resources:

Text Books

1. 'Introduction toembedded systems', K. V.Shibu, TMH education Pvt.Ltd., 2009.
2. 'The Definitive Guide tothe ARM Cortex-M3', Joseph Yiu, Newnes,(Elsevier), 2nd edn, 2010.
3. 'Computer Organization and Design RISC-V Edition', David A. Patterson, John L. Hennessy, Morgan Kaufmann, ISBN: 9780128122761.

Reference Books

1. 'Embedded systems - A contemporary design tool', James K.Peckol, JohnWiley, 2008

Weblinks and Video Lectures (e-Resources):

http://www.digimat.in/nptel/courses/video/106105159/L01.html

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Understand the basic hardware components and their selection methods based on the attributes of Embedded Systems	L2
CO2	Describe the code design process and firmware design approaches	L2
CO3	Acquaint the knowledge of ARM Cortex M3Processor and its salient features	L3
C04	Understand the basics of RISC – V Architecture.	L3
C05	Apply and use Programming Techniques for different End Uses	L3, L4

VLSI INTERCONNECTS			
Course Code	**MVJLVD153**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours

Course objectives:

This course will enable students to:

- Understand the fundamentals of VLSI interconnects
  Analyze the effects of scaling and inductive phenomena in interconnects
- Evaluate advanced RLC interconnect models
- Examine power dissipation and reliability issues in interconnects.
- Investigate cross-talk and timing jitters in coupled interconnects
-

Module-1

Introduction to VLSI Interconnects. Distributed RC interconnect model, Elmore delay, Elmore delay in interconnects, Elmore delay in RC tree and branched interconnects, Equivalent circuit of RC interconnect.

RBT Levels: L2

Module-2

Scaling Effects, Delay mitigation in RC interconnects, Inductive effects in interconnects Distributed RLC Interconnect model (Frequency domain analysis), Transmission line equations. When to consider the inductive, The transfer function of an interconnect, Time-domain response of a lumped model RLC circuit.

RBT Levels: L3

Module-3

Equivalent Elmore model for RLC interconnects (Distributed model), Two-pole model of RLC interconnects from ABCD parameters, Origin of the skin effect, Effective resistance at high frequencies

RBT Levels: L3

Module-4

Power dissipation due to interconnects, Optimum interconnect width for minimizing total power dissipation, Electromigration in interconnects, Mitigation of electromigration. Capacitive coupling in interconnects.

RBT Levels: L3

Module-5

Cross-talk and timing jitters in two identical interconnects, Effects of cross-talk and timing jitters, Techniques for mitigation of cross-talk, Matrix formulation of coupled interconnects. Coupled RLC interconnects, Decoupling of interconnects by diagonalization of matrix

RBT Levels: L3, L4

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements (passed) and earned the credits allotted to each subject/ course if the student secures not less than 50% of the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of 50 Marks.

2. Two assignments each of 20 Marks or one Skill Development Activity of 40 marks to attain the COs and POs.

The sum of three tests, two assignments/skill Development Activities, will be scaled down to 50 marks. CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module.

Suggested Learning Resources:

Text Books:

1. Ashok K. Goel "High-Speed VLSI Interconnections", 2nd Edition, Wiley-IEEE Press, August 2007.
2. S. H. Hall and H.L. Heck, Advanced Signal Integrity for High-Speed Digital Designs, John Wiley & Sons, 2009.
3. Behzad Razavi, Design of Integrated Circuit for Optical Communications, McGraw-Hill, 2003.

Reference Books:

1. H. B. Bakoglu, Circuits, Interconnections, and Packaging for VLSI" Massachusetts: Addison Wesley Publishing Company, 2000.
2. Hall, S.H., G. W. Hall and J. McCall, "High-Speed Digital System Design", First Edition. Wiley Interscience, 2000.

Web links and Video Lectures (e-Resources):

- https://onlinecourses.nptel.ac.in/noc22_ee125/preview
- https://www.youtube.com/watch?v=9HYIuG42a4Y

Semester Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Analyze the distributed RC interconnect model	L3
CO2	Evaluate the impact of scaling and inductive effects in VLSI interconnects, and analyze the time-domain and frequency-domain behavior of distributed RLC models	L4
CO3	Apply advanced RLC interconnect models and determine the effect of high-frequency phenomena	L3
C04	Examine power dissipation, capacitive coupling, and electromigration in interconnects, and apply techniques to optimize interconnect width and ensure reliability.	L2
C05	Analyze cross-talk and timing jitters in coupled interconnects, assess their effects on signal integrity, and apply mitigation techniques using matrix formulations and diagonalization methods	L4

Semester- I

VLSI ARCHITECTURES FOR AI			
Course Code	**MVJLVD154**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- Understand and analyze various fast addition algorithms
- Explore high-speed multiplication techniques
- Comprehend real-number representation and floating-point arithmetic
- Examine advanced implementation techniques.
- Analyze VLSI architectures for neural networks

Module-1

Algorithms for fast addition: Basic addition and counting, Bit-serial and ripple carry adders, Manchester carry chains and adders, Carry-look-ahead adders, Carry determination as prefix computation, Alternative parallel prefix networks, VLSI implementation aspects, Variations in fast adders, Simple carry-skip and Carry select adders, Hybrid adder designs, Optimizations in fast adders, multi-operand addition, Wallace and Dadda trees.

RBT Levels: L2

Module-2

High speed multiplication: Basic multiplication schemes, Shift/add multiplication algorithms, Programmed multiplication, Basic hardware multipliers, Multiplication of signed numbers, Multiplication by constants, Preview of fast multipliers, High radix multipliers, Modified Booth's recoding, Tree and array multipliers, Variations in multipliers.

RBT Levels: L2, L3

Module-3

Real Arithmetic: Representing the real numbers, floating-point arithmetic, The ANSI/IEEE floating point standard, Floating-point arithmetic operations, rounding schemes, Logarithmic number systems, Floating-point adders, Barrel shifter design, Leading-zeros/ones counting, Floating-point multipliers, Floating point dividers, Arithmetic Errors and error control.

RBT Levels: L2, L3

Module-4

Implementation Topics: Computing algorithms, Exponentiation, Approximating functions, Merged arithmetic, Arithmetic by table lookup, Tradeoffs in cost, speed, and accuracy. High-throughput arithmetic, Low-power arithmetic, Fault-tolerant arithmetic, Impact of hardware technology.

RBT Levels: L3, L4

Module-5

VLSI architectures: Analog VLSI neural learning circuits, an analog CMOS implementation of Kohonen network with learning capability, Backpropagation learning algorithms for analog VLSI implementation, Analog implementation of the Boltzmann machine with programmable learning algorithms, VLSI design of the minimum entropy n

RBT Levels: L3, L4

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements (passed) and earned the credits allotted to each subject/ course if the student secures not less than 50% of the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of 50 Marks.
2. Two assignments each of 20 Marks or one Skill Development Activity of 40 marks to attain the COs and POs.

The sum of three tests, two assignments/skill Development Activities, will be scaled down to 50 marks. CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four subquestions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module.

Suggested Learning Resources:

Books

1. Computer Arithmetic (B. Parhami)
2. Digital Arithmetic (M. D. Ercegovac and T. Lang)

Web links and Video Lectures (e-Resources):

- https://onlinecourses.nptel.ac.in/noc22_ee58/preview

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Analyze and implement various fast addition algorithms, for optimized VLSI design	L4
CO2	Evaluate and design high-speed multipliers to achieve efficient arithmetic operations in hardware.	L4
CO3	Apply floating-point arithmetic concepts to design floating-point adders, multipliers, and dividers.	L3
CO4	Design and analyze advanced computation techniques while optimizing tradeoffs between cost, power, speed, and accuracy.	L3,L4
CO5	Evaluate and implement VLSI architectures for neural networks	L4