MVJ COLLEGE OF ENGINEERING
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REPORT

"Advances in 3D MOSFET Architectures: Paving the Way for Next-Generation Semiconductor Scaling"

Date: January 06 – 11, 2025

Institute Name: MVJ College of Engineering, Bangalore

AICTE TRAINING AND LEARNING ACADEMY, PUNE

ATAL FDP (online) on “Advances in 3D MOSFET Architectures: Paving the Way for Next-Generation Semiconductor Scaling”

A Faculty Development Programme (FDP) titled "**Advances in 3D MOSFET Architectures: Paving the Way for Next-Generation Semiconductor Scaling** " *sponsored by AICTE training and Learning (ATAL) Academy* was organized by the Department of Electronics and Communication Engineering. The programme was held from January 6th to 11th, 2025, in the online mode from 6 pm to 9:00pm, on all days except Saturday. On this day, the programme was held from 2pm to 8pm. The event was inaugurated by **Dr Ajayan K R,** Principal, MVJ College of Engineering, Bangalore.

The resource persons for the programme were:

1. **Dr. Roy Paily Palathinkal**, Professor, IIT Guwahati
2. **Mr. Chandrasekhar Kypa,** Vice President & Business Leader, Quest Global, Bangalore
3. **Dr. V. Ramgopal Rao,** Vice-Chancellor, Birla Institute of Technology & Science, Pilani (Former Director, IIT Delhi)
4. **Mr. Sudhakar Reddy Amireddy,** Senior Manager, Intel Corporation, Bangalore
5. **Dr. Harshit Agarwal,** Associate Professor, Indian Institute of Technology, Jodhpur
6. **Dr. Satyabrata Jit**, Professor, Indian Institute of Technology (BHU), Varanasi
7. **Dr. Anish Kumar,** (*Foreign Resource person*), Sr. Staff Engineer, Intel Corporation, Arizona, USA.
8. **Mr. Baranidharan vadivelu**, Application Engineer, Siemens EDA, Bangalore
9. **Dr. Girish Pahwa**, (*Foreign Resource person*), Assistant Professor, National Yang Ming Chiao Tung University, Taiwan

Dr. Roy Paily Palathinkal (Professor, IIT Guwahati)

Education:

- Ph. D., IIT Madras, 2004
- M. Tech, IIT Kanpur, 1996
- B. Tech, College of Engineering Trivandrum, 1990

Experience:

- Professor (Higher Administrative Grade) in Dept. of EEE, IIT Guwahati, from 28-12-2021.
- Professor in Dept. of EEE, IIT Guwahati from 21-04-2012.
- Associate Professor in Dept. of ECE, IIT Guwahati, from 09-08-2007 to 20-04-2012.
- Assistant Professor in Dept. of ECE, IIT Guwahati from 22-07-2004 to 08-08-2007.
- Senior Design Engineer in Magnetic Head Division of Hard Disk Drive Unit at JTS Technology, from 13-03-1996 to 15-03-1999.
- Lecturer at ECE Department SAK Engineering College, University of Bombay, from 12-2-1992 to 23-07-1994.

Mr. Chandrasekhar Kypa (Vice President & Business Leader, Quest Global, Bangalore)

Education:

- M.S. (Software Systems) BITS Pilani, 2003
- Sr. Management Program from IIIM Calcutta, 2014
- PGDBM, XIME Bangalore, 2004

Experience:

- 25+ Years of experience in VLSI Design
- Worked with esteemed organizations like Infineon Technologies, AMD, Philips Semiconductors and Synopsys.

Dr. V. Ramgopal Rao (Vice-Chancellor, Birla Institute of Technology & Science, Pilani) (Former Director, IIT Delhi)

Education:

- B.Tech, Kakatiya University. 1986
- M.Tech., IIT Bombay, 1991
- Ph.D., University of the Bundeswehr, Munich, Germany, 1997

Experience:

- Director, IIT Delhi, 2016-2021
- P. K. Kelkar Chair Professor for Nanotechnology, Department of Electrical Engineering & Chief Investigator for the Centre of Excellence in Nanoelectronics project, IIT Bombay
- Post-doctoral Fellow, University of California, Los Angeles, USA (1997-98)

Mr. Sudhakar Reddy Amireddy (Sr. Manager, Intel Corporation, Bangalore)

Education:

- M. Tech., Indian Institute of Technology, Madras

Experience:

- 25+ years of experience of delivering several generations of server CPU/GPU/Chipset/Wireless/Wireline products and EDA tool development/Design flows.
- He worked at Mentor Graphics, NXP, Infineon and IBM.

Dr. Harshit Agarwal (Associate Professor, Indian Institute of Technology, Jodhpur)

Education:

- Ph. D., Indian Institute of Technology, Kanpur, 2016.
- M. Tech., N.I.T. Hamirpur, 2012
- B. Tech., Birla Institute of Applied Sciences, 2010

Experience:

- Associate Professor, Indian Institute of Technology, Jodhpur, Jun 2023-present
- Assistant Professor, Indian Institute of Technology, Jodhpur, Dec 2019 - Jun 2023
- Post-Doctoral Fellow at the University of California, Berkeley, USA., Oct 2016 - Dec 2019

Dr. Satyabrata Jit (Professor, Indian Institute of Technology (BHU), Varanasi)

Education:

- Ph. D., Indian Institute of Technology (BHU), Varanasi, 2002
- M.Tech., Indian Institute of Technology Kanpur, 1995
- B.E., IIEST, Shibpore, Howrah, 1993

Experience:

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- Associate Professor, Dept. of Electronics Engineering, IIT-BHU, June 2007-June 2010
- Reader, Dept. of Electronics Engineering, IIT-BHU, June 2004-June 2007
- Lecturer, Dept. of Electronics Engineering, IIT-BHU, April 1998-June 2004
- Lecturer, Dept. of Electronics and Comm. Engineering, G.B. Pant Engineering College, Uttaranchal, June 1995-April 1998

Dr. Anish Kumar (Foreign Resource person), Sr. Staff Engineer, Intel Corporation, Arizona, USA

Education:

- Master of Science (Applied Physics), Cochin university of science and technology
- M.Tech., Indian Institute of Technology, Delhi
- Ph.D., Hong Kong University of Science and Technology, Hong Kong.

Experience:

- Staff Engineer, Intel corporation, USA
- Device engineer, Lattice Semiconductor, USA

Mr. Baranidharan Vadivelu (Application Engineer, Siemens EDA, Bangalore)

Education:

- PG diploma in VLSI design after B. Tech in electronics and communication engineering

Experience:

- 20 Years of experience in VLSI domain
- Worked at Graphics, Entuple Technologies

Dr. Girish Pahwa, (Foreign Resource person), Assistant Professor, National Yang Ming Chiao Tung University, Taiwan

Education:

- B.Tech., Delhi Technological University, 2014
- Joint M.Tech. & Ph.D., Indian Institute of Technology, Kanpur, 2020

Experience:

- Assistant Professor, Mar 2024 – Present
- Research Staff: University of California, Berkeley, USA, 2020-2024

ATAL FDP (online) on "Advances in 3D MOSFET Architectures: Paving the Way for Next-Generation Semiconductor Scaling"

The schedule for the Faculty Development Programme is provided below.

MVJ COLLEGE OF ENGINEERING Since 1982

PROGRAMME SCHEDULE

DAY 1 06-01-2025	DAY 2 07-01-2025	DAY 3 08-01-2025	DAY 4 09-01-2025	DAY 5 10-01-2025	DAY 6 11-01-2025
06:00 PM to 06:30 PM Inauguration	06:00 PM – 07:30 PM Session 3 Future directions and trends in 3D MOSFETs-1 Dr. Harshit Agarwal, Associate Professor, IIT, Jodhpur	06:00 PM – 07:30 PM Session 5 Device modeling and TCAD simulation for 3D MOSFETs Dr. Satyabrata Jit, Professor, IIT(BHU), Varanasi	06:00 PM – 07:30 PM Session 7 Parasitic capacitance and resistance in 3D transistors Dr. Satyabrata Jit, Professor, IIT(BHU), Varanasi	06:00 PM – 07:30 PM Session 9 ML driven modelling of semiconductor devices (3D MOSFETs) Dr. Harshit Agarwal, Associate Professor, IIT, Jodhpur	02:00 PM – 03:30 PM Session 11 3D MOSFETs in Post-Moore's Law Era Mr. Baranidharan Vadivelu, Application Engineer, Siemens EDA, Bangalore
06:30 PM – 08:00 PM Session 1 Bottom-up approaches in CMOS Dr. V. Ramgopal Rao, (Former Director, IIT Delhi), Vice-Chancellor, Birla Institute of Technology & Science, Pilani	07:30 PM - 09:00 PM Session 4 The impact of 3D MOSFETs on circuit design and integration-2 Mr. Sudhakar Reddy Amireddy, Sr. Manager, Intel Corporation, Bangalore	07:30 PM – 09:00 PM Session 6 Future directions and trends in 3D MOSFETs-2 Dr. Anish Kumar, Sr. Staff Engineer, Intel Corporation, Arizona, USA	07:30 PM – 09:00 PM Session 8 3D MOSFET applications Dr. Roy Paily Palathinkal, Professor, IIT, Guwahati	07:30 PM – 09:00 PM Session 10 Power and energy efficiency in 3D MOSFETs Dr. Roy Paily Palathinkal, Professor, IIT, Guwahati	03:30 PM – 05:00 PM Session 12 Fabrication technologies for 3D MOSFETs & the impact of 3D MOSFETs on circuit design-3 Mr. Chandrasekhar Kypa, Vice President & Business Leader, Quest Global, Bangalore
08:00 PM – 09:30 PM Session 2 3D MOSFET architectures & the impact of 3D MOSFETs on circuit design-1 Mr. Chandrasekhar Kypa, Vice President & Business Leader, Quest Global, Bangalore					05:00 PM – 06:30 PM Session 13 Challenges in 3D MOSFET realizations Dr. Girish Pahwa, Assistant Professor, National Yang Ming Chiao Tung University, Taiwan
					06:30 PM to 07:30 PM Online test & feedback
					07:30 PM to 08:00 PM Valedictory Session

Inauguration Session:

The Faculty Development Programme (FDP) was inaugurated by **Dr Ajayan K R**, Principal, MVJ College of Engineering, Bangalore on 6th January 2025. The principal addressed the participants and congratulated them on registering for this FDP. The participants of this FDP are faculty from the host institution, faculty from other colleges, and professionals from the industry.

The list of approved participants is as follows:

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Day 01 (06-01-2025) - Session 1 - "Bottom-up Approaches in CMOS" | Dr. V. Ramgopal Rao, Vice-Chancellor, Birla Institute of Technology & Science, Pilani (Former Director, IIT Delhi)

Dr. V. Ramgopal Rao began his presentation by highlighting the importance of enhancing the performance of MOSFET devices to achieve a PPA (performance, power, and area) advantage. The speaker then moved on to explain the role that a self-assembled monolayer (SAM) can play in a MOSFET. He elaborated that a Porphyrin Self-Assembled Monolayer can improve the performance of a MOSFET in the following ways:

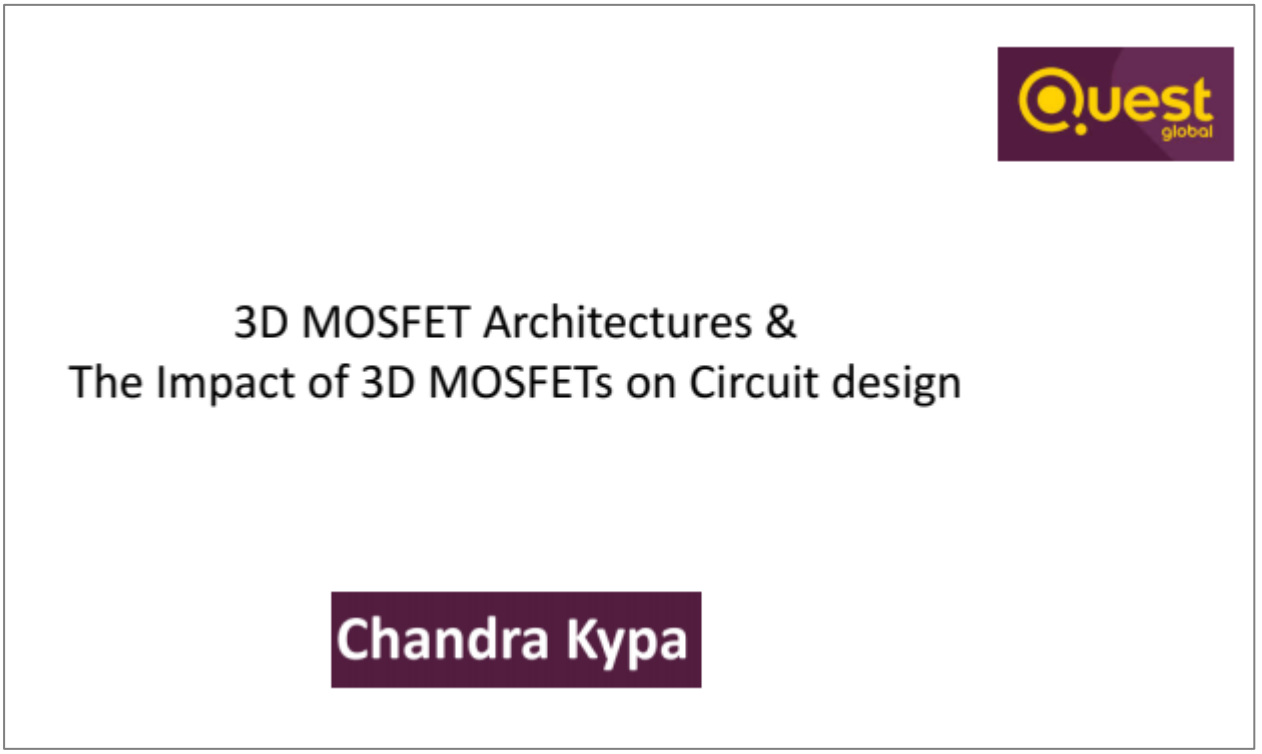
(a) It can act as a barrier to copper diffusion.

(b) It can enhance the ON/OFF current ratio.

(c) It can modify the threshold voltage.

Dr. V. Ramgopal Rao concluded his session with an important observation: While the semiconductor industry is currently utilizing 2-3 nm technology nodes with devices such as FinFET and GaaFET, conducting research in these areas at the academic level is challenging. This is primarily due to the high costs associated with setting up labs capable of fabricating devices with such small geometries. He suggested that, at the college level, faculty should focus on materials research and explore how different materials can influence device performance.

Day 01 (06-01-2025) - Session 2 - "3D MOSFET Architectures & The Impact of 3D MOSFETs on Circuit design-1" | Mr. Chandrasekhar Kypa**,** Vice President & Business Leader, Quest Global, Bangalore



Mr. Chandrasekhar Kypa began the session by posing the question of why FinFET devices are required. The speaker then described the device architectures of MOSFETs and FinFETs, highlighting their advantages over planar MOSFETs.

From a circuit design perspective using FinFETs, Mr. Kypa began by highlighting the advantages of incorporating FinFET technology into circuit design. He then discussed the challenges associated with circuit design using FinFETs. The main challenges include: (1) The effective transistor size in FinFET circuits is quantized, (2) The lack of body bias, and (3) The presence of higher parasitic effects.

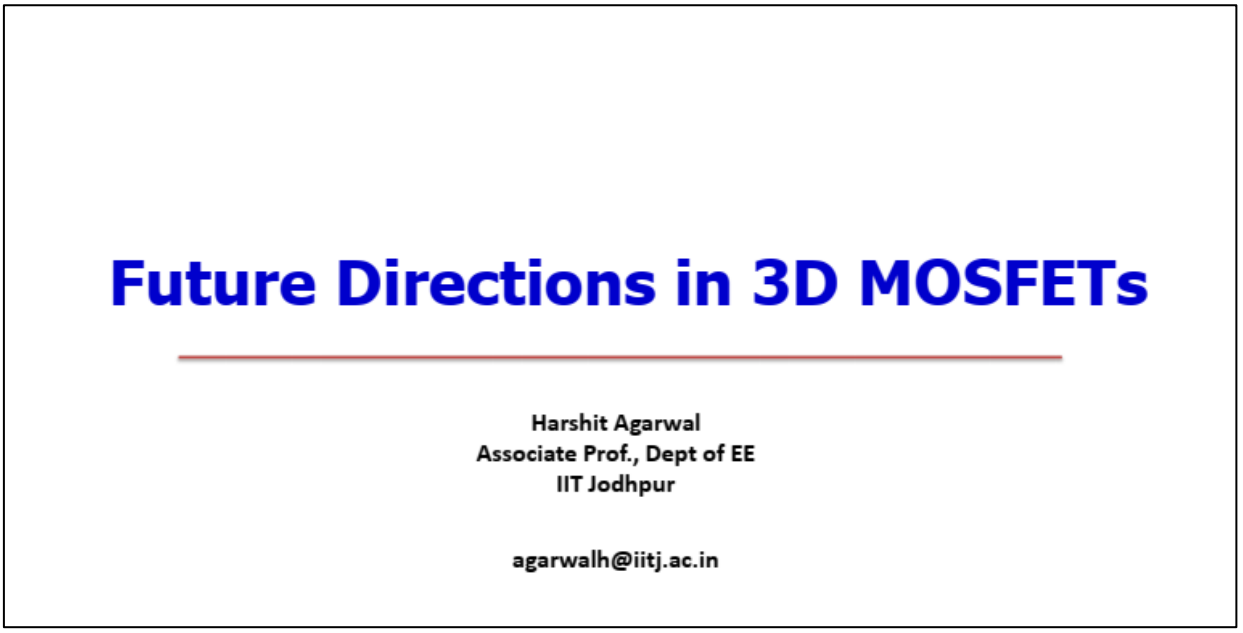
Key takeaways from this session are:

(1) FinFETs are useful where density and speed are critical.

(2) FinFETs are not ideal for analog designs, which require customized W/L ratios.

(3) FinFETs are not ideal for SRAM designs, as they exhibit higher leakage compared to planar transistors.

Day 02 (07-01-25) - Session 3 -"Future Directions and Trends in 3D MOSFETs" | Dr. Harshit Agarwal, Associate Professor, Indian Institute of Technology, Jodhpur



Dr. Harshit Agarwal began the session by explaining the fundamental principles of improving speed and power in a circuit.

Maximum circuit speed can be obtained by (1) increasing the ON current and (2) reducing the capacitance. The on-current can be increased by Power can be reduced by reducing the (1) supply voltage. (2) Off current and (3) capacitance.

The maximum circuit speed can be achieved by (1) increasing the ON current and (2) reducing the capacitance. The ON current can be increased by doing the following things: (a) channel strain engineering, (b) high-k dielectric, (c) decrease channel length.

Power can be reduced by (1) lowering the supply voltage, (2) reducing the OFF current, and (3) minimizing the capacitance.

Next, the speaker moved on to FinFET devices and then discussed future directions in 3D MOSFETs, focusing on the Gate-All-Around FET (GaaFET). He explained the concept of vertically stacking nMOS and pMOS devices.

Day 02 (07-01-25) - Session 4 -" The Impact of 3D MOSFETs on Circuit design and Integration" – | Mr. Sudhakar Reddy Amireddy, Senior Manager, Intel Corporation, Bangalore

Mr. Sudhakar Reddy began by discussing 42 years of microprocessor trends and then explained the growing demand for smaller transistors to achieve improved speed and reduced area. This demand has driven the development of new device structures and advanced fabrication technologies.

The speaker then compared the device structures of planar MOSFETs, FinFETs, and GAA FETs. He noted that Intel is leading the next era of computing through advancements in transistor and packaging innovations.

From the circuit perspective, he discussed the following key points: (1) the design steps involved in circuit design, (2) the VLSI design flow, and (3) the standard cell architecture for planar/FinFET technologies and the associated layout differences.

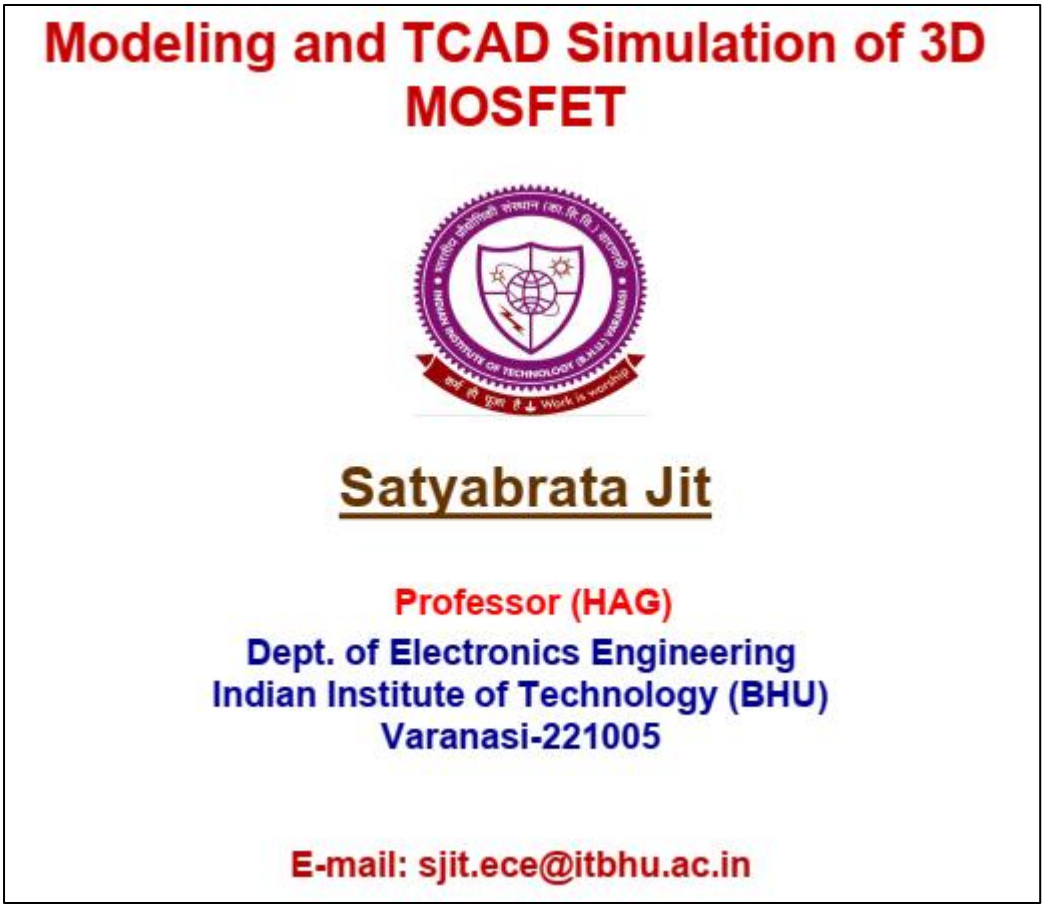
Mr. Sudhakar Reddy concluded the session with the following points related to 3D MOSFETs.

(1) 3D MOSFETs offer improved performance, enhanced power efficiency, and greater scalability.

(2) 3D MOSFETs play a crucial role in advancing VLSI design at nanoscale dimensions.

(3) 3D MOSFETs pave the way for future innovations in semiconductor technology

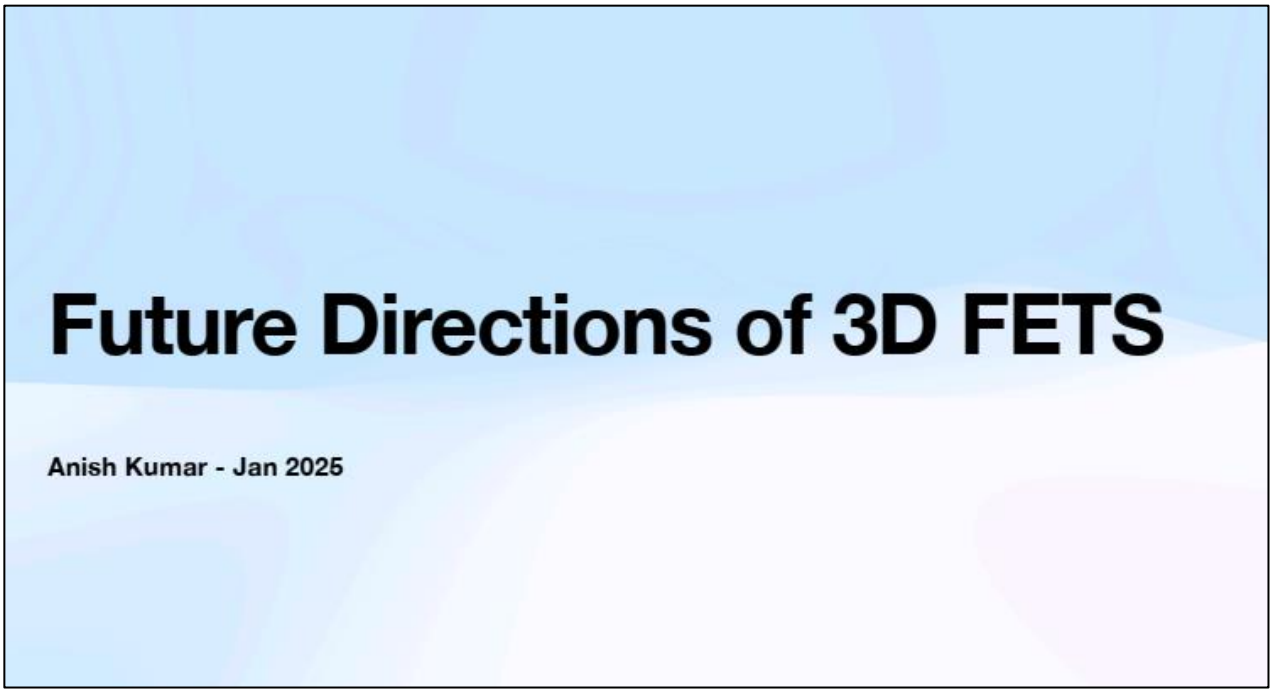
Day 03 (08-01-25) - Session 5 - "Device Modeling and TCAD Simulation for 3D MOSFETs" | Dr. Satyabrata Jit, Professor, IIT(BHU), Varanasi



Dr. Satyabrata Jit began the session by explaining the operating principles of planar MOSFETs and modeling their basic I-V characteristics. The speaker then moved on to the modeling of significant short-channel effects, including VT roll-off, drain-induced barrier lowering (DIBL), gate leakage current caused by tunneling through the gate oxide, and the increase in subthreshold current (Ioff) with a decrease in channel length.

The speaker concluded the session by mentioning two commonly used TCAD device simulation tools, Silvaco ATLAS TCAD and Synopsys TCAD. He also emphasized the crucial point that TCAD tools must be calibrated by comparing simulation data with experimental data available for similar devices in the literature.

Day 03 (08-01-25) - Session 6 - "**Future Directions and Trends in 3D MOSFETs"** | Dr. Anish Kumar (Foreign Resource person), Sr. Staff Engineer, Intel Corporation, Arizona, USA.



Dr. Anish Kumar started the session by describing semiconductor technology trends, beginning with Moore's Law, new materials, and advanced packaging. He mentioned that Intel expects to have one trillion transistors by 2030.

He explained the pros and cons of front-side and back-side power delivery in chips. On the packaging side, Dr. Anish discussed different packaging techniques such as FCBGA 2D, EMIB 2.5D, FOVEROS, and EMIB 3.5D. He also elaborated on several reliability aspects related to Gate-all-around Field Effect Transistors (GaaFET).

Dr. Kumar also highlighted the importance of thermal management in semiconductor devices, emphasizing the need for efficient heat dissipation techniques to ensure optimal performance and reliability.

Dr. Kumar concluded his session by addressing the future of semiconductor technology, including the potential impact of artificial intelligence (AI) and machine learning (ML) on the design and optimization of semiconductor devices. He stressed the importance of interdisciplinary collaboration and continuous innovation to drive the next wave of technological breakthroughs.

Day 04 (09-01-25) - Session 7 - "Parasitic Capacitance and Resistance in 3D Transistors" | Dr. Satyabrata Jit, Professor, IIT (BHU), Varanasi

Dr. Satyabrata Jit explained different types of scaling in the semiconductor industry – constant field scaling, constant voltage scaling, and generalized scaling. He also highlighted the impact of both oxide thickness reduction and channel length reduction on device performance.

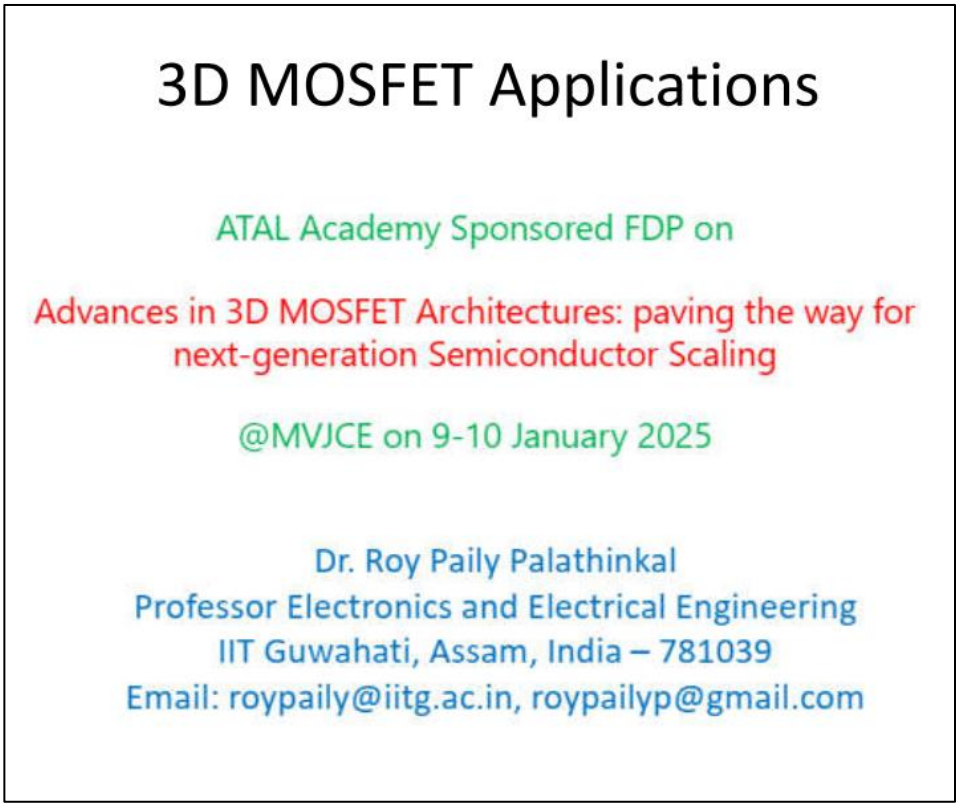
Next, the speaker moved on to parasitic capacitance and resistance in 3D MOSFETs (FinFET and GaaFET) and their impact on device performance.

Parasitic capacitance and resistance are critical factors in determining the performance and scaling limits of 3D transistors, such as FinFETs and Gate-All-Around FETs (GaaFETs). These parameters directly affect the speed, power consumption, and reliability of modern semiconductor devices.

Increased gate wrapping in 3D structures like FinFETs and Gaa FETs enhances electrostatic control but can lead to higher gate-to-drain/source capacitance. Fringe Capacitance is more pronounced in 3D geometries due to the non-planar structure. The Parasitic capacitance slows down the transistor switching speed (increases RC delay) and also contributes to dynamic power dissipation

Understanding and managing parasitic capacitance and resistance is crucial to the continued scaling and performance improvement of 3D transistors. Innovations in materials, device architecture, and fabrication techniques are key to overcoming these challenges.

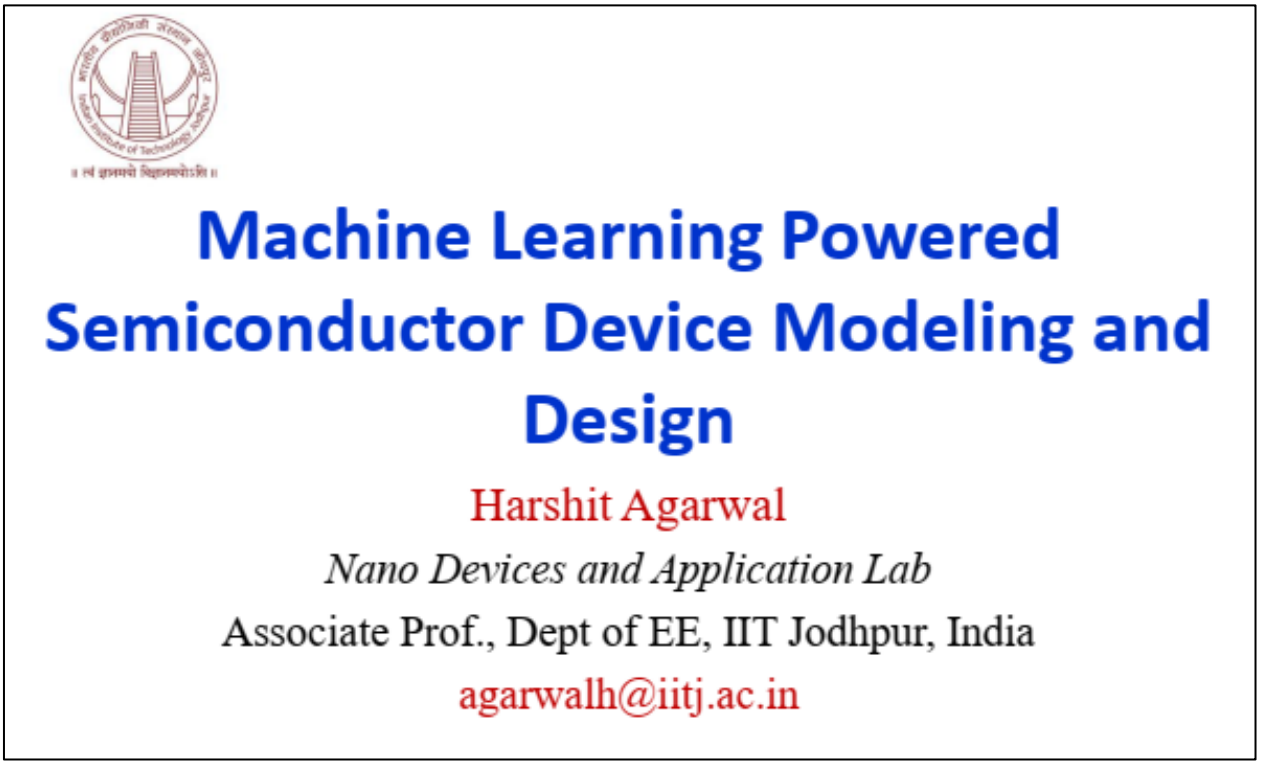
Day 04 (09-01-25) - Session 8 - "**3D MOSFET Applications"** | Dr. Roy Paily Palathinkal, Professor, IIT, Guwahati



Dr. Roy started the session by comparing planar MOSFETs with three-dimensional (3D) MOSFETs, such as FinFETs and Gate-All-Around (GAA) FETs. These devices have become integral to modern semiconductor technology and are ideal for various applications, particularly in advanced digital systems.

- 3D MOSFETs are essential in processors and GPUs for high-performance computing due to their high drive current, and energy efficiency
- 3D MOSFETs are widely used in smartphones, tablets, and wearable devices where energy efficiency and compactness are critical
- IoT devices require ultra-low-power operation, making 3D MOSFETs suitable
- 3D MOSFETs are used in automotive electronics, especially in advanced driver-assistance systems (ADAS) and electric vehicle (EV) power management.

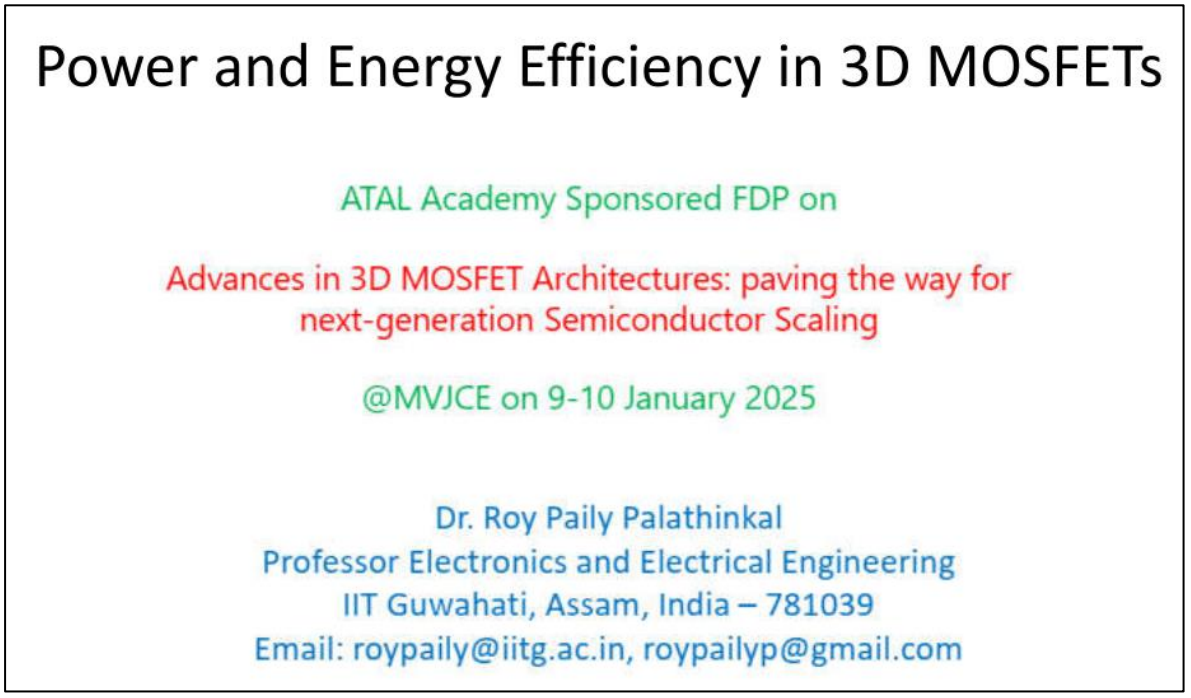
Day 05 (10-01-25) - Session 9 - "**ML driven modelling of semiconductor devices (3D MOSFETs)" |** Dr. Harshit Agarwal, Associate Professor, Indian Institute of Technology, Jodhpur



Dr. Harshit Agarwal first explained the importance of compact models for the semiconductor devices. If 1,000 transistors are fabricated on a chip, not all of them will exhibit the same I-V characteristics. Using this example, the speaker introduced the concept of "variability." This variability can be modeled by incorporating changes in doping concentration, as well as variations in L, W, tox, etc. Next, he discussed variability modeling.

Dr. Harshit Agarwal also discussed testing methodology and key challenges in ML-driven modeling of semiconductor devices.

Day 05 (10-01-25) - Session 10 - "Power and Energy Efficiency in 3D MOSFETs" | Dr. Roy Paily Palathinkal, Professor, IIT, Guwahati



Dr. Roy explained the dynamic and static power dissipation in 3D MOSFETs and their dependence on various parameters. Energy efficiency focuses on minimizing the energy consumed per operation and is closely tied to power consumption.

Applications benefiting from power and energy efficiency include (1) mobile devices, data centers, IoT devices, wearables, and health monitors.

3D MOSFETs, such as FinFETs and Gate-All-Around (GAA) FETs, provide significant improvements in power and energy efficiency compared to planar MOSFETs. Their superior electrostatic control and advanced design reduce power dissipation and enhance performance, making them ideal for modern applications.

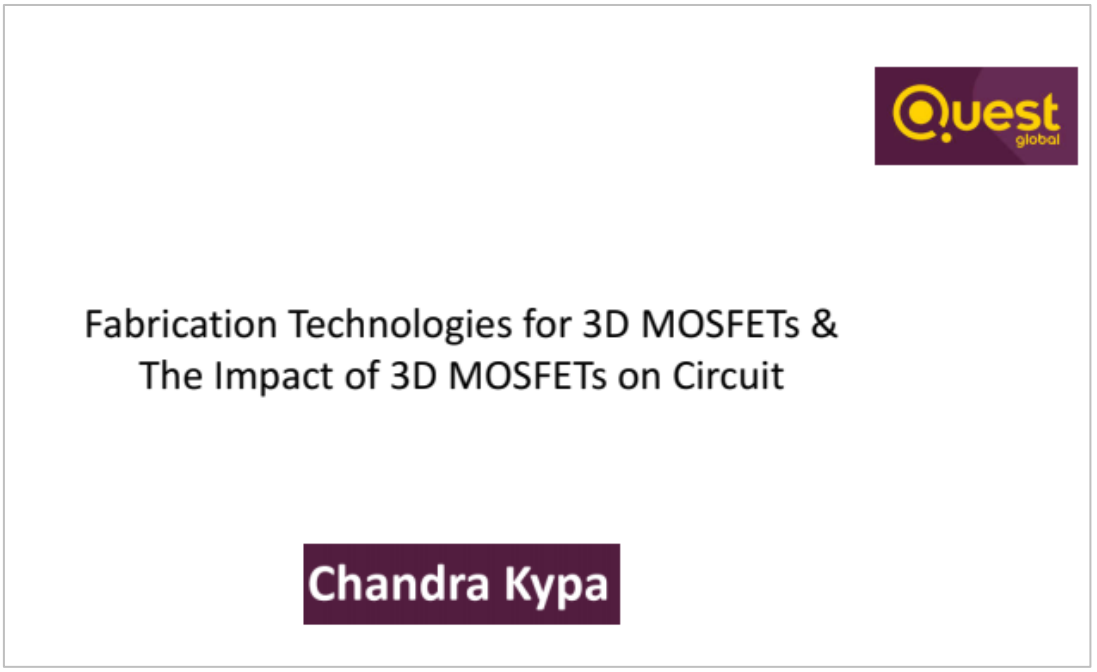
Day 06 (11-01-25) - Session 11 - "3D MOSFETs in Post-Moore's Law Era" | Mr. Baranidharan Vadivelu,
Application Engineer, Siemens EDA, Bangalore

Mr. Baranidharan Vadivelu began the session by describing the basic structure of a planar MOSFET and then explaining Moore's Law. He also discussed the limitations of traditional MOSFET devices.

The speaker then described the structure of 3D MOSFETs, specifically the Gate-All-Around Field Effect Transistor (GAA-FET), and highlighted its advantages over planar MOSFETs.

The limitations and challenges associated with 3D MOSFETs were also discussed.

Day 06 (11-01-2025) - Session 12 - "Fabrication Technologies for 3D MOSFETs & The Impact of 3D MOSFETs on Circuit design" | Mr. Chandrasekhar Kypa**,**
Vice President & Business Leader, Quest Global, Bangalore



Mr. Chandrasekhar Kypa began the session by describing the fabrication process of a planar MOSFET. He then explained the steps involved in fabricating a FinFET device. In FinFET fabrication, the critical process step is the creation of extremely thin "fins" that extend upward from the substrate. These "fins' are the active channel regions of the FinFET. The fins are created using a process such as photolithography and etching, ensuring that the fins have precise dimensions for efficient device performance.

The performance of a FinFET can be improved in three main ways: strain engineering, the use of high-kkk dielectrics, and reducing the channel length.

(1) The strain engineering involves applying mechanical strain to enhance the channel carrier mobility. Tensile stress improves nMOS performance whereas compressive stress improves pMOS.

(2) Hgih-k dielectrics enable thicker oxides so that gate leakage can be minimized

Regarding the layout, Mr. Kypa highlighted that the design rules for FinFETs differ from those for planar MOSFETs, particularly because of the 3D nature of the structure. FinFET layouts require more advanced design rules for sidewall spacing, gate-to-fin overlap, and other dimensions to ensure proper functioning at smaller nodes.

Day 06 (11-01-2025) - Session 13 - "Challenges in 3D MOSFET realizations" | Dr. Girish Pahwa, National Yang Ming Chiao Tung University, Taiwan

Dr. Girish began the session by highlighting emerging applications of 3D MOSFETs, with a particular focus on "Edge Computing." He outlined the key requirements for edge computing as follows:

1. High-performance transistors to process the vast amounts of sensor data
2. Low power consumption due to a limited power budget
3. Compact size to accommodate space constraints
4. Large memory bandwidth to efficiently store and access extensive data

The technological challenge lies in the fact that frequency does not increase with transistor scaling due to the inability to remove the generated heat. Consequently, new materials, devices, and computing schemes are being explored. The evolution of device structures has shifted from planar to 3D innovations.

Dr. Girsh described the device structures of both FinFET and GaaFET, followed by a detailed explanation of the process flow for nanosheet GaaFET. As the number of sheets increases, the drive current also increases. A maximum of seven sheets has been demonstrated experimentally. Additionally, smaller sheet spacing reduces parasitic C_{gd} and source/drain resistance.

The speaker concluded the session with the following takeaways.

- AI and emerging applications need energy-efficient and high-performance 3D FET device technologies
- There has been huge progress in realizing Nanosheet FETs; however, process, geometry, and thermal challenges remain
- 3D vertical CFETs with significant area savings are the next technology down the roadmap

Online test, feedback and Valedictory session

After the 13th session, an online test was conducted, followed by a feedback session. The online FDP concluded with a valedictory session.

Conclusion:

In conclusion, the 6-day online Faculty Development Programme (FDP), sponsored by ATAL Academy, provided a valuable platform for participants to enhance their research capabilities in the field of 3D MOSFETs. The active engagement of the participants demonstrated their keen interest in staying abreast of the latest advancements FinFET and GaaFET technology, as well as the potential applications of these devices based devices in AI and emerging applications.

Outcome of the FDP:

A total of 90 participants, including faculty members from the host institution, faculty from other colleges, and professionals from the industry, actively participated in the online ATAL FDP. This programme provided a valuable learning experience for all attendees, offering them the opportunity to interact with resource persons and discuss their research initiatives.