Report on the Guest Lecture

"Application-Specific Integrated Circuit (ASIC) Flow for Chip Manufacturing"

Date of the Event	28/03/2025
Title of the Event and Lecture	**Application-Specific Integrated Circuit (ASIC) Flow for Chip Manufacturing**
Name of the Resource Speaker	Mr. Deepu Alex
Number of Participants	75
Venue	Seminar Hall 5/2 (Room No 33)

A Guest Lecture on the topic "**ASIC flow for chip manufacturing**" was organized at MVJ College of Engineering on 28th March 2025, providing students with a platform to explore cutting-edge ASIC technology for chip design. The event brought together students, faculty, and industry professionals to discuss advancements in **ASIC** technologies and explore opportunities related to projects, internships, and careers.

The Chief Guest for the session was Mr. Deepu Alex, Senior Principal DFT Engineer at Ampere, Bangalore, India. His insights into **ASIC** applications, industry trends, and career pathways enriched the participants' understanding of this rapidly evolving domain.

Objectives of the Guest Lecture

- To enhance knowledge and skills in ASIC technology for chip design.
- To foster collaborations between students, faculty, and industry experts.
- To provide insights into career opportunities, internships, and industry projects in the field of ASIC.

Event Overview

The Guest Lecture on "**ASIC flow for chip manufacturing** " was organized by the Department of VLSI Design Engineering on 28th March 2025. The event was presided over by Dr. Rameshan Kariyadan, Senior Professor of the Department (VLSI), with Mr. Deepu Alex, Senior Principal DFT Engineer at Ampere, Bangalore, India, as the Chief Guest. The welcome address was delivered by our VKLSI 4th SEM students Mr, Channaya and Miss Akshata, and the session took place at Seminar Hall – 2 (room no. 33) from 10:00 AM to 1:00 PM.

Mr**. Deepu Alex**, an expert in the **ASIC** domain, delivered an insightful lecture that provided a comprehensive overview of **ASIC** technology and its critical role in chip design. He provided an in-depth understanding of ASIC technology and its advantages over Field-Programmable Gate Arrays (FPGAs), highlighting its superior performance, power efficiency, and area optimization. He elaborated on the ASIC design flow, beginning with specification development, where chip functionalities are defined. He then explained the process of Register Transfer Level (RTL) design using hardware description languages like Verilog. Design for Functional Verification Testability (DFT) was discussed in detail, where he introduced tools like ModelSim and VCS used for testbench development and simulation.

The session also covered synthesis, which involves converting RTL code into a gate-level netlist using Electronic Design Automation (EDA) tools such as Synopsys Design Compiler. Mr. Alex explained the importance of Design for Testability (DFT) techniques, including scan chains and built-in self-test (BIST), ensuring proper functionality during fabrication. He then moved on to physical design, covering floor planning, placement, routing, and optimization using tools like Cadence Innovus. The final steps of signoff, including timing analysis (STA), power analysis, and manufacturing rule checks like Design Rule Check (DRC) and Layout Versus Schematic (LVS), were discussed before the chip is sent for fabrication. He also highlighted the significance of packaging and testing to ensure the functionality and reliability of the final chip.

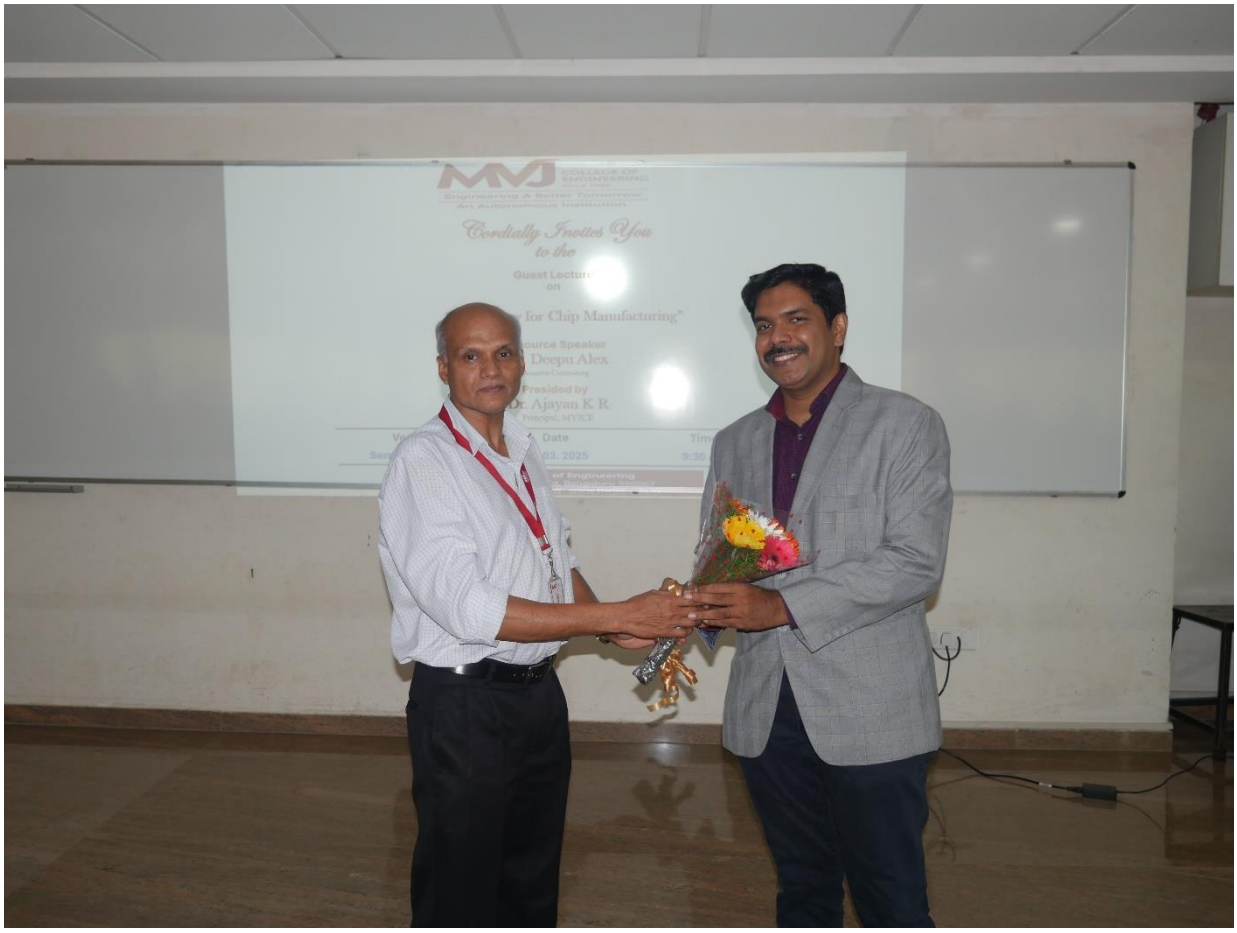
The lecture concluded with a stimulating Q&A session, where students and faculty members engaged in discussions on real-world ASIC design challenges, career opportunities in the semiconductor industry, and emerging technological advancements. The session was formally concluded with a vote of thanks delivered by one of our VLSI students Miss Jyotshna, who expressed gratitude to the guest speaker, the organizing committee, and the participants for their active involvement.

The lecture provided students with a clear understanding of the ASIC design and manufacturing process while exposing them to industry-standard tools and workflows. It also encouraged students to explore career opportunities in VLSI design and the semiconductor industry. The event was highly informative and interactive, equipping attendees with valuable technical knowledge and industry insights into ASIC design.

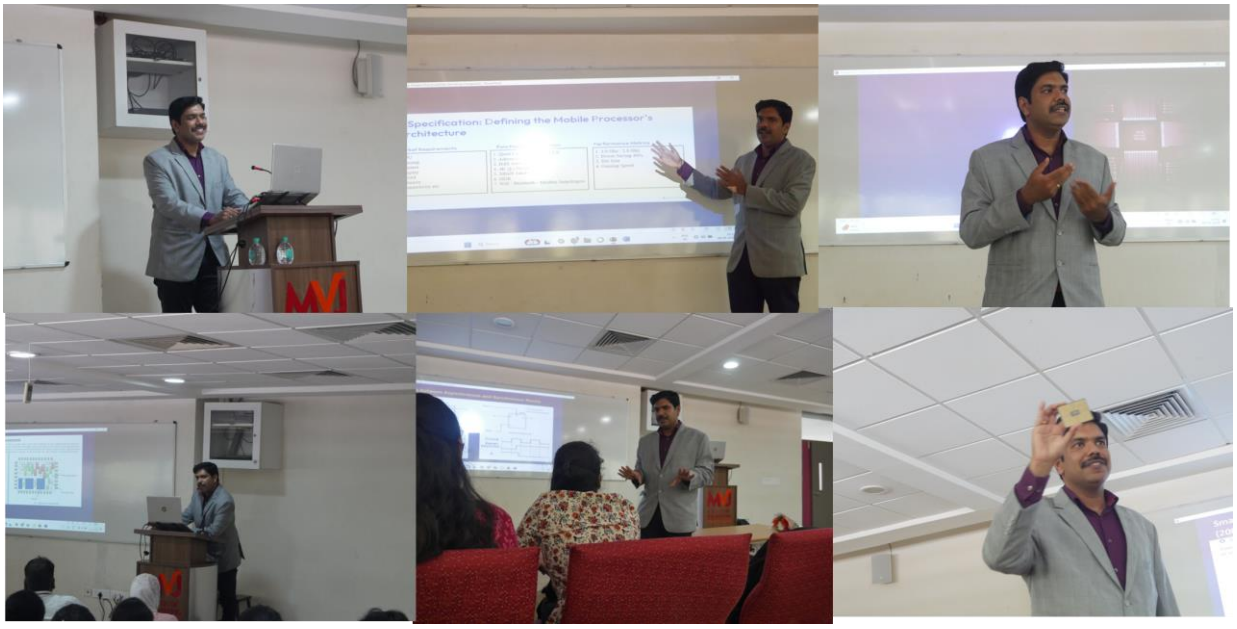
Acknowledgments

Special thanks to **Mr. Deepu Alex** for his inspiring presence and valuable insights. We also extend our gratitude to **Shri M J Balachndar M** and **Dr. Ajayan K. R. and Dr. Shima Ramesh Maniyath** for their continuous support. The organizing team appreciates the efforts of **coordinators, faculty mentors, sponsors, and students** for their contributions to the success of

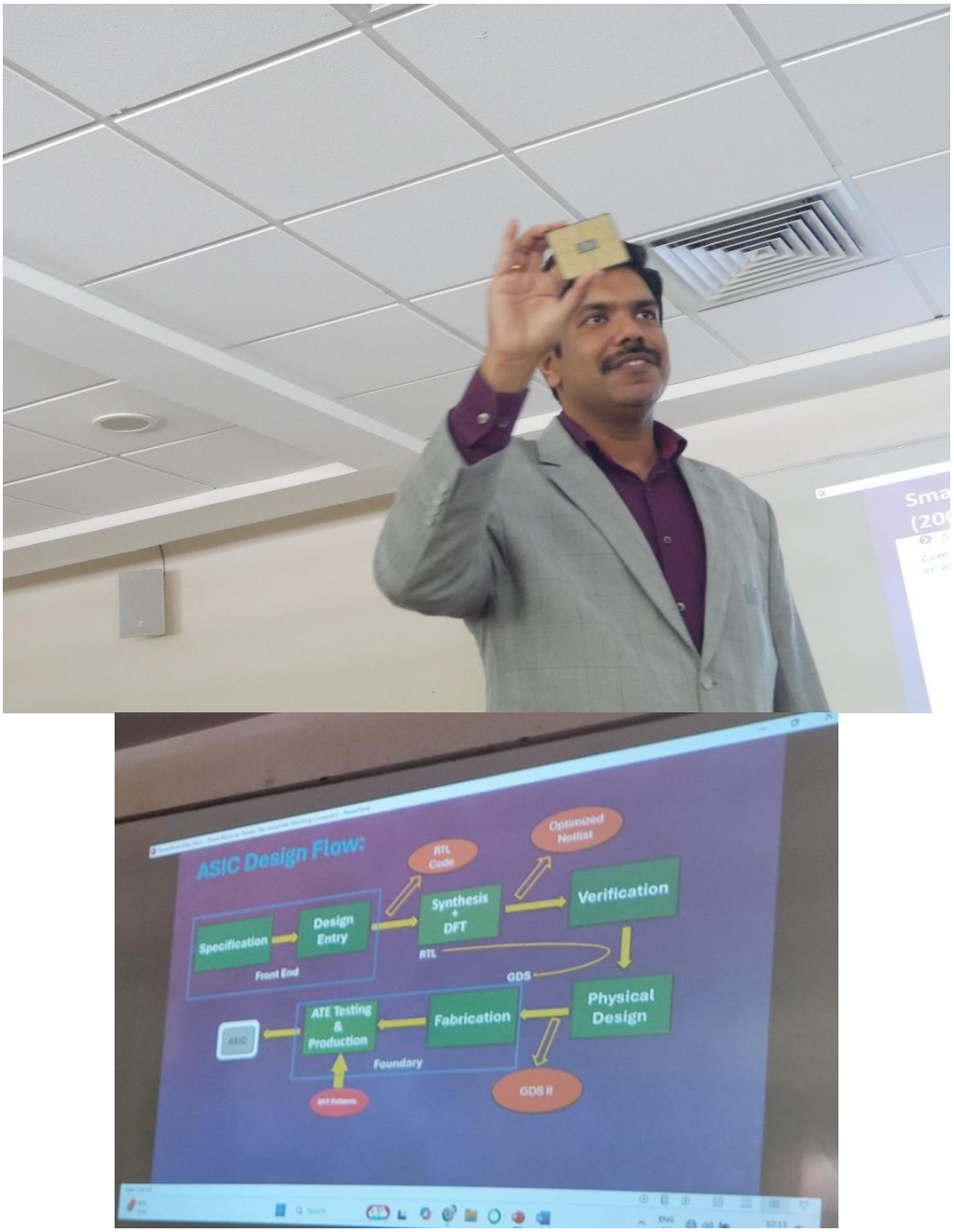
this event.



Dr. Rameshan Kardiyan welcoming the chief guest Shri Deepu Alex.

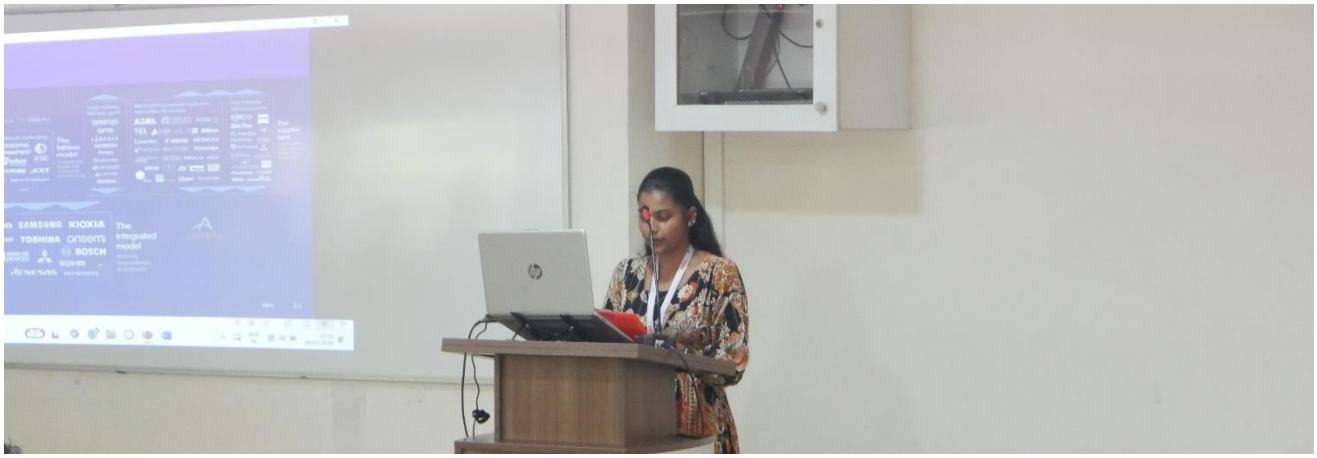


Lecture by the speaker.



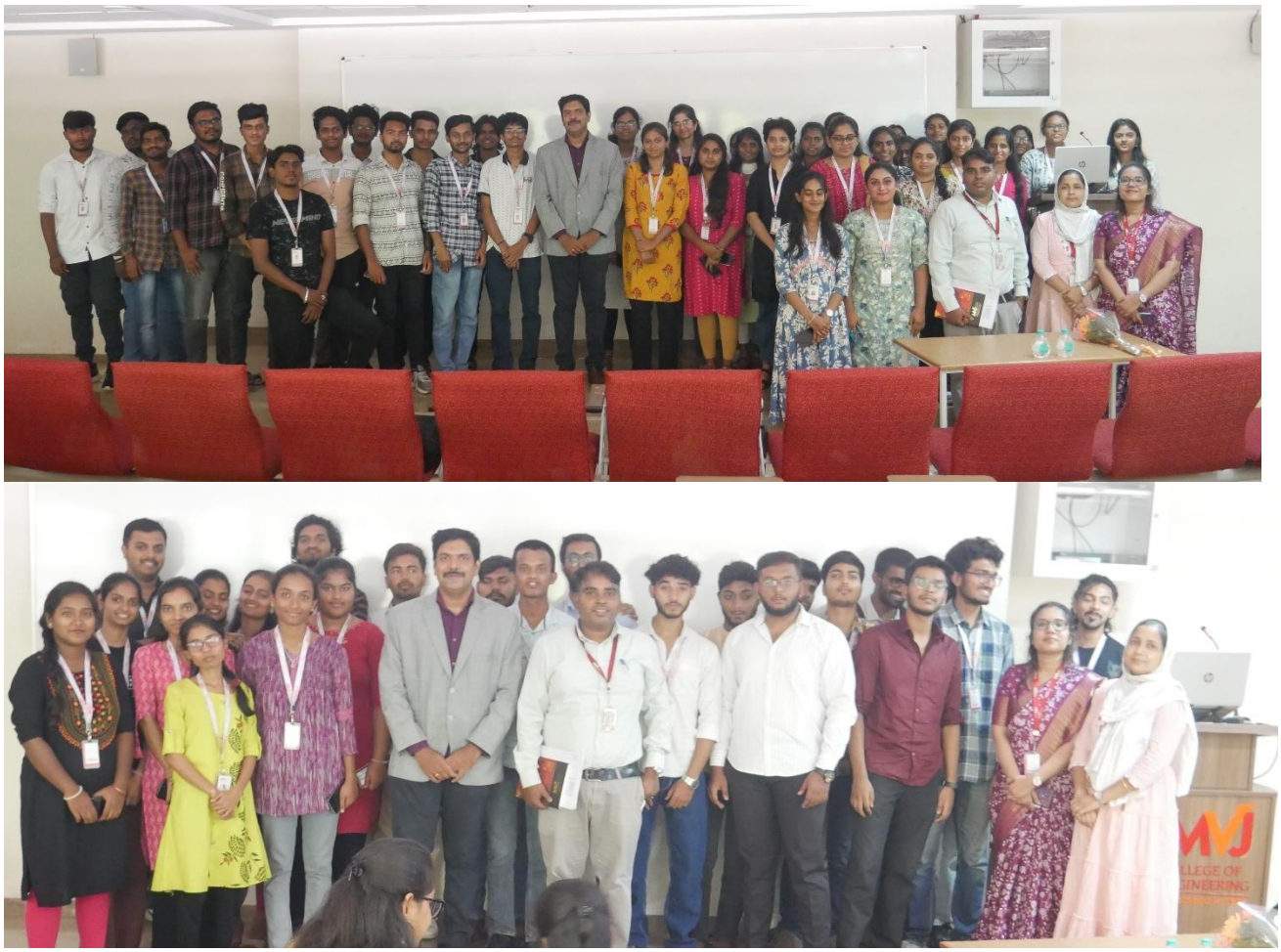
Speaker showing an IC circuit board related to ASIC process.

Participants' interactions with the speaker during and after the lecture.



Vote of thanks conveyed by Miss Jyotsna.

Participants during the lecture.



Group photo with a few students and faculty members.