MVJ COLLEGE OF ENGINEERING
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# Report

# on

# Two Days STTPs on

# "Tiny SoC: Designing and Verification of Controller and Memory using System Verilog"

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| **Date of the Event** | 26/03/2025-27/03/2025 |
| **Title of the Event and Lecture** | **A Tiny SoC: Designing and Verification of Controller and Memory using System Verilog** |
| **Name of the Resource Speaker** | Mr. Shaikh Aleem Ur Rehaman<br>Mr. Shaikh Asadur Rehaman |
| **Number of Participants** | 40 |
| **Venue** | HDL LAB (Room No 334) |

A **Short-Term Training Program (STTP)** titled ***" A Tiny SoC: Designing and Verification of Controller and Memory using System Verilog"*** was organized at MVJ College of Engineering from 26th to 27th March 2025. The event served as a platform for students to explore key concepts in chip design and verification, fostering engagement between academia and industry. It brought together students, faculty members, and industry professionals to discuss the significance of chip verification and explore potential opportunities for projects, internships, and careers in the semiconductor industry.

The Chief Guests for the sessions were:

- **Mr. Shaik Aleem Ur Rehaman, ASIC Engineer at Microsoft India**
- **Mr. Shaikh Asadur Rehaman, Design and Verification Engineer at Alpha Semiconductors**

Both experts specialize in Application-Specific Integrated Circuit (ASIC) design and verification. They are currently working on cutting-edge System-on-Chip (SoC) technologies, which are in high demand in the current semiconductor job market.

Their insightful sessions on verification techniques, coupled with engaging delivery, were highly appreciated by participants. The discussions on industry trends and career pathways further enriched the participants' understanding of the evolving VLSI domain.

## Objectives of the STTP:

- To gain hands-on experience in SoC architecture design and hardware implementation.
- To gain the verilog-based verification skills for system level verifications.
- Boosts the colleges and industry collaboration towards the job opportunities.

## Event Overview

The two-day STTP was conducted by the **Department of VLSI Design Engineering**, presided over by **Dr. Namita**, HoD of the VLSI Department, and **Dr. Rajesh Saha**, Assistant Professor. The sessions were led by the esteemed Chief Guests, Mr. Aleem and Mr. Asadur Rehaman.

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**Day 1:**

The event began with a welcome address delivered by UG-VLSI students, **Ms. Hemapriya** and **Mr. Naveen**. Sessions were held at the HDL Lab (Room No. 334) from 10:10 AM to 3:55 PM.

- **Mr. Aleem**, with over 9 years of industry experience, presented an in-depth session on ALU design and verification along with hands on. He guided students through conventional ALU verification methods, common types of verification errors, and their resolution. He also explained System Verilog constructs such as $urandom and $urandom_range, which help improve testbench efficiency.
- **Mr. Asadur**, from Alpha Semiconductors, delivered a session on memory controller verification using Verilog. He provided personalized guidance to students in writing efficient verification code and introduced them to **EDA Playground**, a cloud-based, open-source simulation tool.

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**Day 2:**

The second day began at 10:35 AM with a recap of the previous day's sessions and doubt clearing.

- The experts then introduced the **architecture of microprocessors**, emphasizing the role and importance of the ALU in processor operations.
- Mr. Asadur illustrated the concept of **pipelining** using relatable real-life examples, such as stages in cooking, to demonstrate the performance benefits of pipelining in processor design (e.g., increased throughput).
- A detailed session followed on **memory design and verification**, linking the topic back to ALU for continuity. Students were asked to design a 64*8 bit memory and

develop a corresponding testbench.

- In the evening, the session transitioned to **communication protocols**, particularly focusing on the **SPI protocol**. The speakers highlighted its industrial relevance and usage in communication between discrete ICs.

Beyond the technical knowledge, Mr. Aleem and Mr. Asadur emphasized the growing demand and career opportunities in the field of design verification within the semiconductor industry.

The event concluded with a **vote of thanks** by **Dr. Rajesh Saha**, who expressed sincere gratitude to the speakers, organizers, and participants for their enthusiastic involvement and contributions.

## Acknowledgments

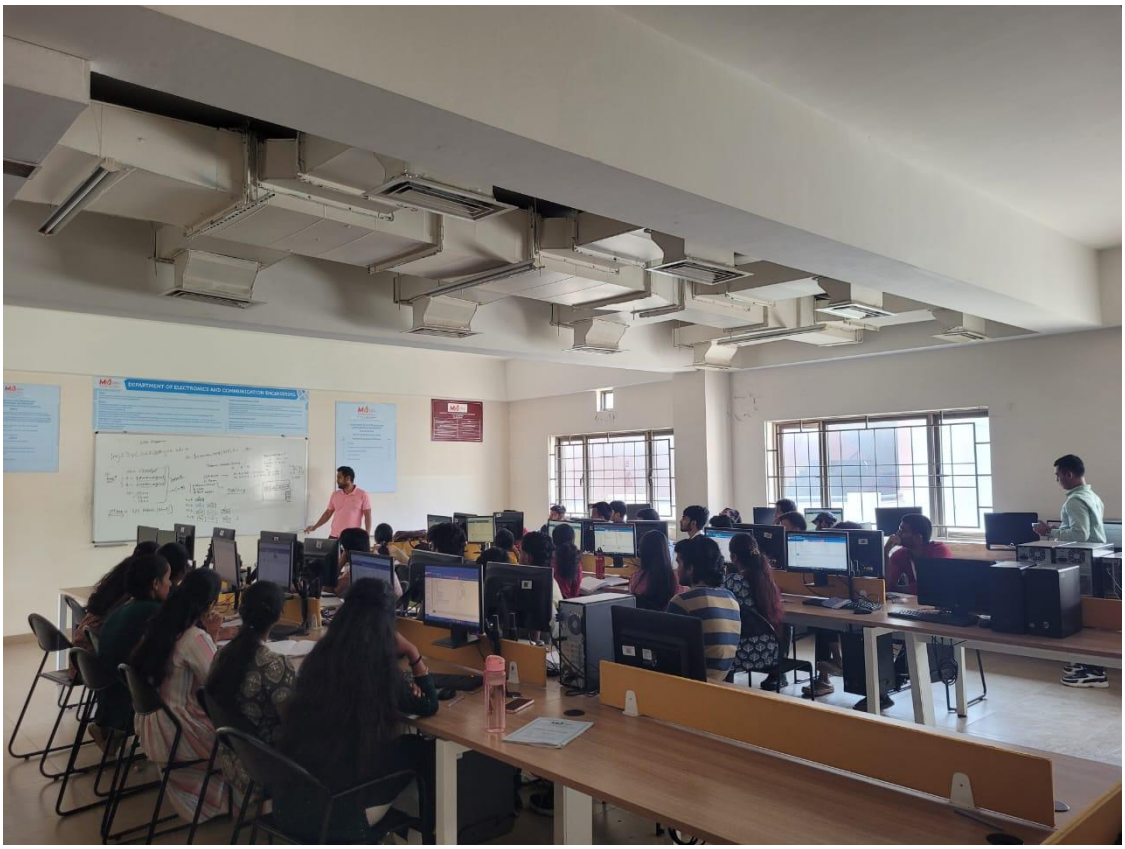
Special thanks to **Mr. Shaikh Aleem Ur Rehaman and Mr. Shaikh Asadur Rehaman** for their inspiring presence and valuable insights. We also extend our gratitude to **Shri M J Balachndar M** and **Dr. Ajayan K. R., Dr. Shima Ramesh Maniyath** and **Dr. Namita** for their continuous support. The organizing team appreciates the efforts of **coordinators, faculty members and students** for their contributions to the success of this event.

**Dr. Namita**, **welcoming chief guest** Mr. Shaikh Asadur Rehaman

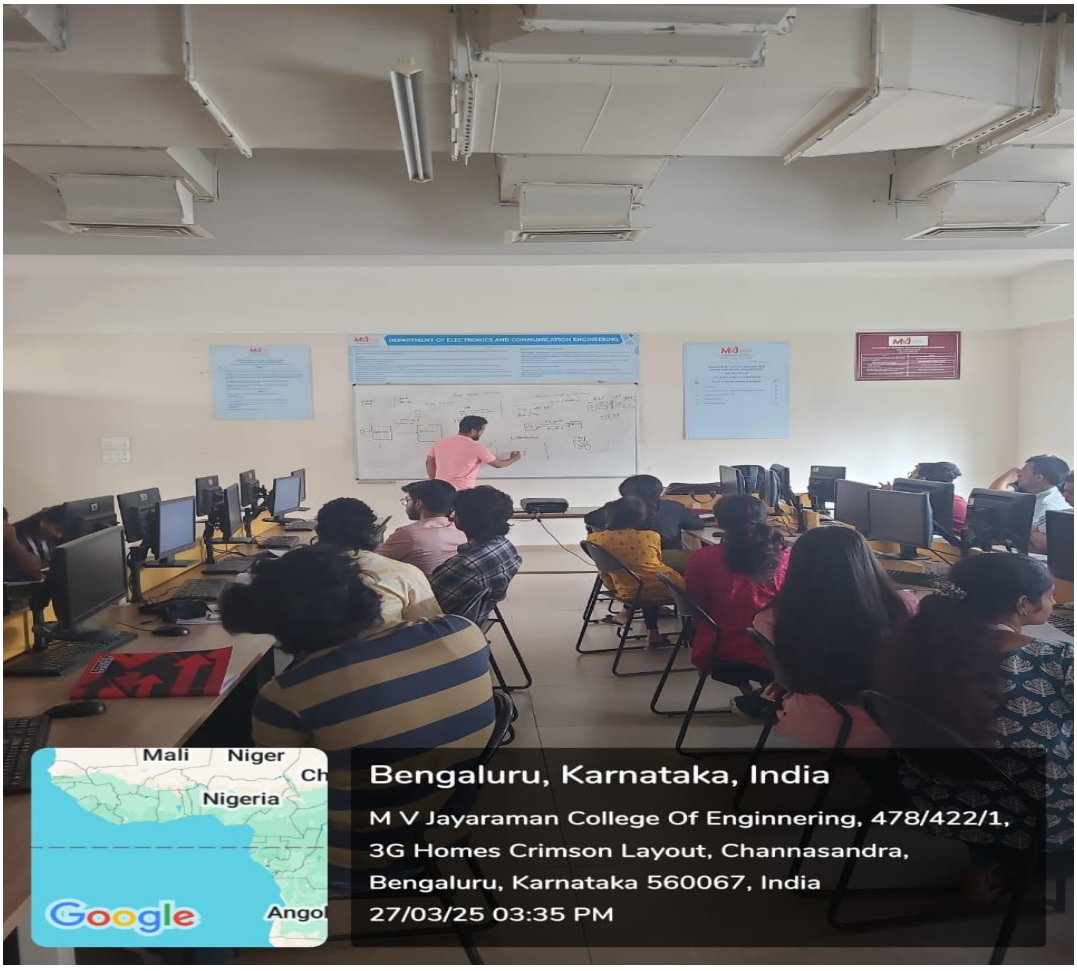
**Dr. Rajesh Saha**, **welcoming chief guest** Mr. Shaikh Aleem Ur Rehaman


**Lecture by the speaker on Day1**


**Speakers' interactions with students in Day1**

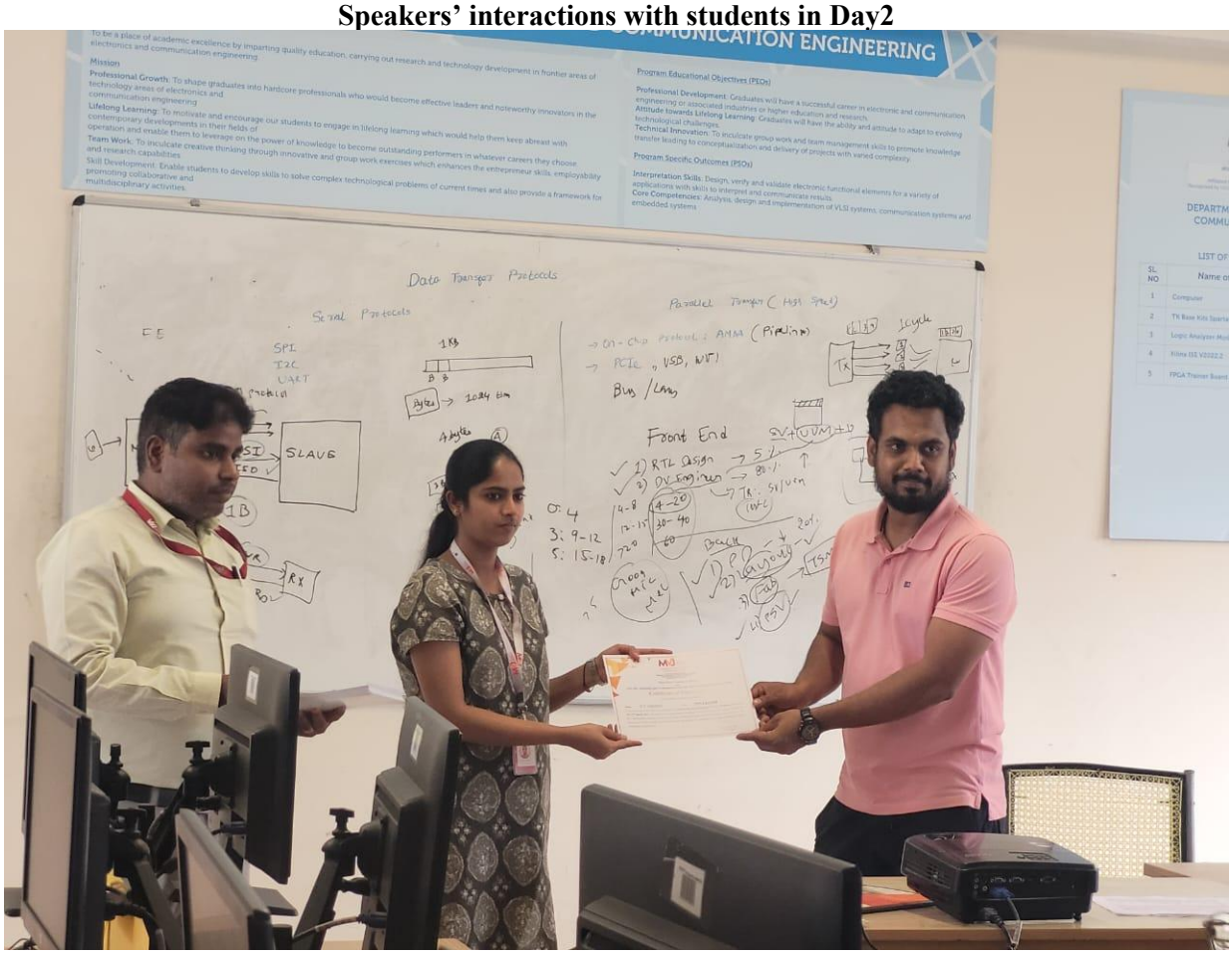


**Lecture by the speaker on Day2**



**Lecture by the speaker on Day2**


**Speakers' interactions with students in Day2**




**Certificate Distribution**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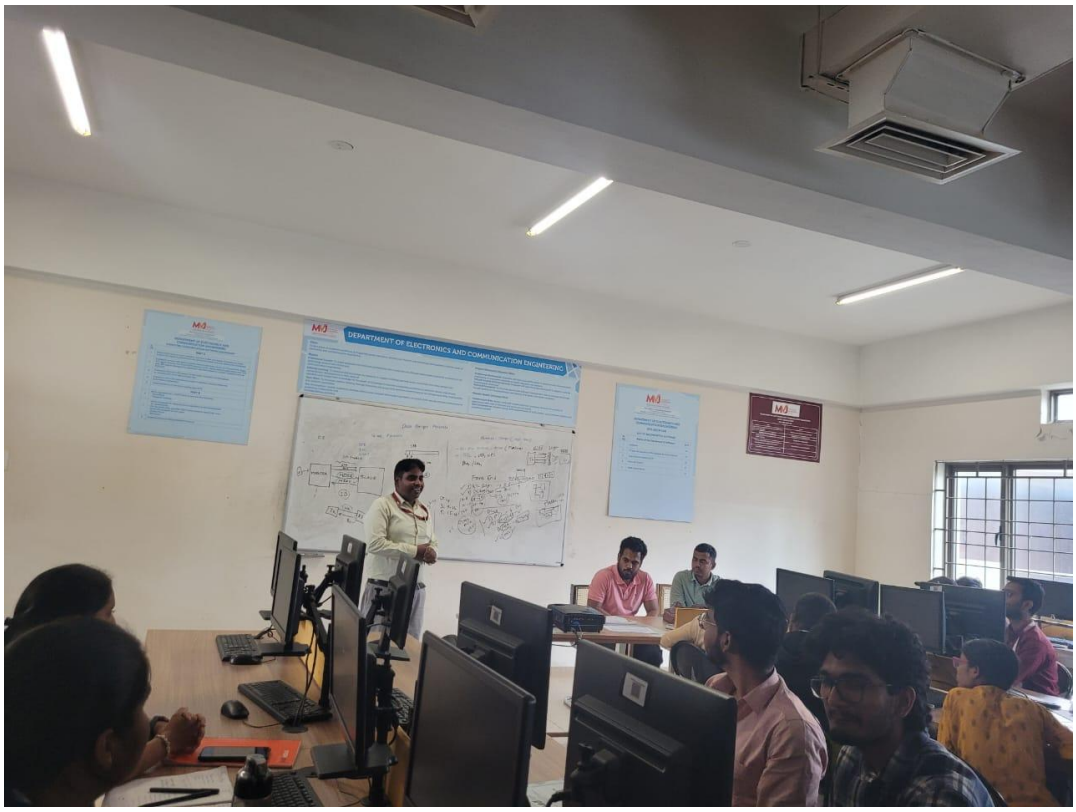


**Vote of thanks conveyed by Dr. Rajesh Saha**