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Report on the Club Activity "Verilog Quest: A Competitive Digital Design Challenge"

The department of VLSI Design and Technology conducted a Club Activity titled Verilog Quest: A Competitive Digital Design Challenge on 23-08-2025 from 1:30 PM to 3:30 PM. in Room No. 334.

Objectives of the Event

The primary objectives of the event were:

- Strengthen participants' understanding of digital design principles.
- Promote hands-on experience in Verilog coding and simulation.
- Encourage problem-solving and innovation through circuit implementation.

Event Overview

The event began in Room No. 334. The problem was defined by the chief guest, Mr.Danish Patil, and the participants (studets) engaged in "The design of a counter that counts odd numbers, considering numbers from 1 to 7". The participants showed keen interest, and were in a competitive mindset to achieve success.



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Figure 1: Students performing the club activity problem



(a) Winning Team



(b) Second winning team

Figure 2: (a) Winning team, and (b) Second winning team with the guest judge

Day	Time	Session Details
Saturday, August 23 2025	1:30 - 1:40 pm 1:40 - 3:20 pm 3:20 - 3:30 pm	Rules, Guidelines, and Tool Setup Instructions Design Challenge Evaluation and Results

Table 1: Schedule of the Event



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Outcomes and Impact

Participants engaged in a series of challenges, including the design of arithmetic logic units and custom logic circuits using Verilog. They implemented and simulated their designs using industry-standard tools, Vivado and implemented them in an FPGA Board.

The key takeaways from this event are:

- Students acquired practical skills in digital circuit design by implementing Verilogbased projects on FPGA boards using Vivado, gaining exposure to real-world hardware workflows and industry-standard development environments.
- The activity equipped students with foundational expertise in HDL coding, simulation, and hardware deployment—key competencies for careers in VLSI design, embedded systems, and semiconductor engineering.

Conclusions

Verilog Quest was a hands-on digital design competition focused on enhancing students' skills in Verilog HDL and FPGA implementation. Participants designed and simulated circuits using Vivado and deployed them on FPGA boards, gaining practical exposure to industry-standard workflows. The event featured Mr. Dinesh Patil, Director of RD at Synopsys, who shared valuable insights into semiconductor innovation and leadership. Students developed technical competence, problem-solving abilities, and teamwork, preparing them for careers in VLSI and embedded systems.

Report by: Dr. Rabaya Basori

Affiliation: Faculty in the Department of ECE (VLSI Design).

MVJ College of Engineering