MVJ COLLEGE OF ENGINEERING
Since 1982
Engineering A Better Tomorrow

An Autonomous Institute
Approved by AICTE, New Delhi
Affiliated to VTU, Belagavi
Recognized by UGC under 2(f) & 12(B)
Accredited by NBA & NAAC

Two Days STTP on "Digital System Design using Altera FPGA"

The department of **Electronics and Communication Engineering** conducted a two-day STTP titled **Digital System Design using Altera FPGA"** on **date in 26-09-2025 to 27-09-2025** at **10.30 am**, in **Seminar hall 4**.

The inaugural day of the Short-Term Training Programme (STTP) on "Digital System Design using Altera FPGA", organised by the Department of Electronics and Communication Engineering, MVJ College of Engineering, was held on September 26, 2025, with enthusiastic participation from around 61 registered students. The event commenced at 10:30 AM with a warm welcome address by Dr. Shima Ramesh Maniyath, Head of the ECE Department, who also felicitated the resource person, Mr. Padmanaban Kalyanaraman, Software Enabling and Optimisation Engineer at Intel, CEG. The session began with an insightful overview of FPGA technology, its architecture, and its diverse applications in various industries, including automotive, broadcast, entertainment, instrumentation, and networking.

Objectives of the Event

The primary objective of this Short-Term Training Programme is to provide participants with a comprehensive understanding of FPGA technology and its practical applications in digital system design. The event aims to:

1. Introduce the fundamentals of FPGA architecture and its role in modern electronics and embedded systems.
2. Familiarise students with Hardware Description Languages (HDL) such as Verilog, VHDL, and System Verilog, and their use in modelling digital circuits.
3. Demonstrate the complete FPGA design flow, including creation, constraint application, compilation, timing closure, and device configuration.
4. Provide hands-on experience using Quartus Prime Design Software, enabling students to create, simulate, and implement digital designs on FPGA hardware.

5. Bridge the gap between theoretical knowledge and industry practices, by exposing students to real-world tools and workflows used in FPGA-based system development.
6. Encourage practical learning through lab sessions, focusing on basic digital designs like switch-to-LED, memory modules, and multipliers.
7. Highlight the versatility and reprogrammability of FPGAs, showcasing their applications across domains such as automotive, broadcast, instrumentation, and networking.
8. Inspire students to explore career opportunities in hardware design, embedded systems, and FPGA development through interaction with industry experts.

Event Overview

The event flow of the inaugural day of the STTP on "Digital System Design using Altera FPGA" was structured to provide a balanced mix of theoretical insights and practical exposure. The programme began with a formal inauguration ceremony at 10:30 AM, where Dr Shima Ramesh Maniyath, Head of the ECE Department, welcomed the participants and felicitated the resource person, Mr Padmanaban Kalyanaraman, Software Enabling and Optimisation Engineer from Intel, CEG. Following the inauguration, the first session introduced students to the fundamentals of FPGA, including its architecture, applications, and relevance in modern electronics. This was followed by a detailed explanation of Hardware Description Languages (HDL) such as Verilog, VHDL, and System Verilog, highlighting their concurrent nature and differences from conventional programming languages.

The next segment focused on the FPGA design flow, emphasising the five key stages: Create, Constrain, Compile, Close Timing, and Configure. Participants were then guided through the Quartus Prime Design Software, exploring its editions, user interface, and essential tools like the IP catalogue, RTL viewer, and pin planner. The afternoon sessions were dedicated to hands-on lab activities, where students implemented basic digital designs such as a switch-to-LED circuit, memory modules, and multipliers using HDL templates and IP blocks. Throughout the day, students engaged actively with the resource person, asking questions and participating in

real-time demonstrations. The event concluded with a deeper understanding of FPGA-based system design and programming, setting a strong foundation for the subsequent sessions of the STTP.

Demonstrating the two-day STTP, the sessions showcased immersive, hands-on applications where participants applied digital system design concepts using Altera FPGA boards.

Figure 1 highlights the moment of appreciation and respect as the HOD presents a bouquet to the Intel engineer, marking the start of a collaborative learning experience.

Figure 1: Dr Shima Ramesh Maniyath Felicitating Mr Padmanaban Kalyanaraman

Figures 2 and 3 show the engaged audience of 61 students attentively listening to the introductory talk, reflecting their enthusiasm and interest in FPGA technology.

Figure 2: Participants Attending the Opening Session

Figure 3: Introduction to FPGA Architecture and Applications

Figure 4 highlights the process of designing arithmetic circuits using HDL templates,

demonstrating the flexibility and power of FPGA-based computation. Figure 5 em-

Figure 4: Hands-on Lab Session – Switch to LED Design

phasises the STTP's role in transforming classroom learning into **industry-relevant skills**, making students more competent and confident in applying their knowledge to real-world problems

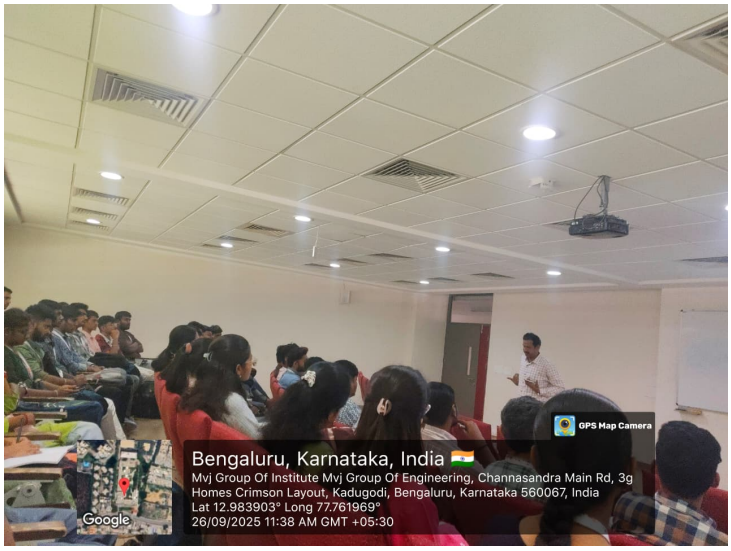

Figure 5: **Bridge the gap between theoretical knowledge and industry practices**, by exposing students to real-world tools and workflows used in FPGA-based system development.

Figure 6: Hands-on session in progress: participants working on Altera FPGA boards on day 2

Figure 6 shows participants actively engaged in the hands-on session on Altera FPGA development, exploring real-time digital system design and implementation under expert guidance on day 2.

The event also had a strong impact on student engagement and skill development. Through interactive sessions and lab activities, participants were able to bridge the gap between academic concepts and real-world applications. The exposure to Intel's FPGA ecosystem and guidance from an industry expert provided valuable insights into current trends and career opportunities in embedded systems and hardware design.

Moreover, the STTP fostered a collaborative learning environment that encouraged peer interaction and active participation. The practical sessions on switch-to-LED circuits, memory modules, and multipliers helped students internalise design principles and understand the importance of synthesis, fitting, and device programming. Overall, the event contributed to building a strong foundation in digital system design and inspired students to pursue further learning and innovation in the field of programmable logic and embedded technologies.

.

Figure 7: Group Photo – STTP on Digital System Design using Altera FPGA

Conclusions

The STTP successfully met its objectives by enhancing students' technical skills, bridging academic learning with industry practices, and inspiring interest in FPGA-based development. The event laid a strong foundation for future exploration in embedded systems and digital design, making a meaningful impact on the participants' academic and professional growth.

Report by: Dr. Shima Ramesh Maniyath

Affiliation: HOD, Department of Electronics and Communication Engineering,

MVJ College of Engineering