MVJ COLLEGE OF ENGINEERING
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Report on the Guest Lecture "Design of Modern AI and Cloud CPU Processors"

The department of **VLSI Design and Technology** conducted a **Guest Lecture** titled **Design of Modern AI and Cloud CPU Processors** on **12-11-2025** at **11:00 AM to 01:00 PM**, in **Seminar Hall 1**.

Objectives of the Event

The primary objectives of the event were:

- Understand architectural innovations in AI and cloud CPU design.
- Explore integration of accelerators like GPUs, TPUs, and NPUs.
- Discuss power efficiency, scalability, and security in processor design.

Event Overview

The session on "Design of Modern AI and Cloud CPU Processors" featured Mr Anil Kumar Baratam, a distinguished digital design leader currently associated with Ampere India. With vast experience in logic cell design, advanced circuit architectures for CPUs, GPUs, and NPUs, and cutting-edge 3nm process technologies, Mr Baratam has made remarkable contributions to next-generation semiconductor innovation. In this event, he provided a comprehensive exploration of how modern CPU architectures are evolving to meet the demands of AI and cloud computing workloads. He discussed the design philosophies behind energy-efficient, high-performance, and scalable processors, highlighting the integration of specialised hardware accelerators such as GPUs, TPUs, and NPUs. The session attracted VLSI students, faculty members, and research enthusiasts, offering valuable insights into processor architecture, hardware acceleration, and real-world chip design practices. Mr Baratam's multidisciplinary perspective spanning EDA-RTL co-optimisation, circuit design, and microarchitecture offered participants a rare opportunity to understand the depth and breadth of AI-centric hardware design in the semiconductor industry.

Welcome Address

A student from the VLSI Dept. Srushti, given a welcome address for the event.

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Figure 1: Welcome Address

0.1 Guest Lecture session

Figure 2 shows the picture of students and faculty with the resource person (2a) and the resource person taking a lecture (2b).

(a) Group photo with a few students and faculty members.

(b) Lecture by the speaker

Figure 2

Day	Time	Session Details
Wednesday, November 12 2025	11.00 - 11.10 am 11.10 - 01.00 pm	Welcome Address Guest Lecture

Table 1: Schedule of the Event

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Outcomes and Impact

- Technical Insight into AI and Cloud CPU Design: Mr Baratam explained how processor architectures are being redefined to support massive AI workloads in cloud environments. He discussed the role of heterogeneous computing and hardware acceleration in achieving performance scalability and efficiency.

- Integration of Accelerators: The talk emphasised how GPUs, TPUs, and NPUs are integrated within modern CPU ecosystems to optimise AI training and inference, bridging the gap between software frameworks and hardware implementations.
- Industry Exposure and Career Pathways: Drawing from his experience at Ampere India and TSMC, Mr Baratam shared insights into real-world semiconductor workflows and discussed opportunities for internships, research collaborations, and advanced studies in VLSI and AI hardware design.

- Future Vision: The session concluded with an engaging discussion on the future of AI-centric processors, emphasising the growing importance of collaboration between hardware and software design teams to drive the next wave of innovation in computing architecture.

Conclusions

The lecture ended with a dynamic Q&A session, where students and faculty engaged with Mr Baratam on topics ranging from career opportunities in AI and cloud CPU design.

Report by: Assistant Prof. Anusree R

Affiliation: Faculty in the Department of VLSI Design and Technology.

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