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3-Day FDP on "Next Generation Communication and Computing: From Massive MIMO to AI Acceleration on FPGA"

The **Department of Electronics and Communication Engineering**, in collaboration with **ECE (ACT), ECE (VLSI), and IIoT Department**, successfully organised a **three-day Faculty Development Program (FDP)** on "Next Generation Communication and Computing: From Massive MIMO to AI Acceleration on FPGA" from **8th, 9th, and 12th January 2026**, between **10:00 AM and 4:00 PM**. The event was held in **Seminar Hall 2** and witnessed enthusiastic participation from **around 35 faculty members**. The program featured expert sessions on cutting-edge topics in wireless communication and computing, complemented by **hands-on training sessions conducted by CoreEL Technologies** in **Lab Rooms 203 and 334**, ensuring participants gained both theoretical insights and practical experience.

Objectives of the Event

- The primary objective of this FDP was to provide faculty members and participants with an in-depth understanding of next-generation communication technologies and computing paradigms. The program aimed to bridge the gap between theoretical concepts and practical implementations in areas such as Massive MIMO, intelligent surfaces, AI-driven wireless communication, and FPGA-based acceleration. It also sought to equip participants with hands-on experience using industry-standard tools like MATLAB, Simulink, and Xilinx Vivado.

Event Overview

Day 1 began with an insightful forenoon session by **Dr. Sushrutha**, **Associate Dean RV University**, focusing on the fundamentals of antenna arrays and beamforming. Dr.Shima Ramesh Maniyath , HOD of the ECE Department, delivered the welcome address. The session started at 10.00 am. Antenna-on-Chip technology, voltage and current behavior in electric fields, and the skin effect at frequencies above 2 GHz. Maxwell's equations were discussed to explain the relationship between electric and magnetic fields, followed by an introduction to Phase-Locked Loops (PLL)

and their role in synchronisation. The evolution of mobile network technologies from early generations to 5G and 6G was highlighted, along with beam formation techniques for narrowband and wideband systems. The derivation of the array factor for two isotropic point sources was explained, and concepts of beam steering and formation were demonstrated through the speaker's project work. The session also introduced generic and optimum beamformers, including the MVDR beamformer, and concluded with insights into the latest Wi-Fi technologies (Wi-Fi 6 and 7) and channel estimation techniques.

Dr. Rameshan, Professor, ECE Department, presenting a bouquet to Dr. Shushrutha during the inaugural session of Day 1.

Figure 1: Dr. Shushrutha delivering an insightful session on "Fundamentals of Antenna Arrays and Beamforming" during Day 1 of the FDP

Figure 2: Dr. Shushrutha engaging participants with an in-depth discussion on advanced beamforming techniques and antenna array fundamentals.

Session 2 by **Dr. Trupti Sagar** explored the transition "From Antennas to Intelligent Surfaces," bridging the gap between fundamental antenna theory and modern wireless systems. The session traced the evolution of wireless communication from SISO to intelligent surfaces and provided an overview of SISO, SIMO, MISO, and MIMO configurations. Topics included antenna arrays, linear array phase shift models, spatial filtering, and massive MIMO antenna systems. The concept of IRS/RIS (Intelligent/Reconfigurable Intelligent Surfaces) was introduced, along with diversity versus spatial multiplexing and interpretation of MIMO channel matrices. Capacity gain was explained through Shannon's perspective, and practical aspects of MIMO in 4G and 5G networks were discussed, including mmWave technology. The session concluded with emerging trends such as AI integration with FPGA for intelligent wireless systems and research directions like RIS channel modeling, joint BS-RIS optimisation, hardware non-idealities, real-time FPGA implementation, and AI-driven MIMO control.

Figure 3: Dr. Shima Ramesh, HOD of ECE Department, presenting a bouquet to Dr. Trupti Sagar before the commencement of Session 2 on Day 1 of the FDP

Figure 4: Dr. Trupti Sagar delivering an engaging session on "From Antennas to Intelligent Surfaces: The Expanding Role of MIMO" during Day 1 of the FDP

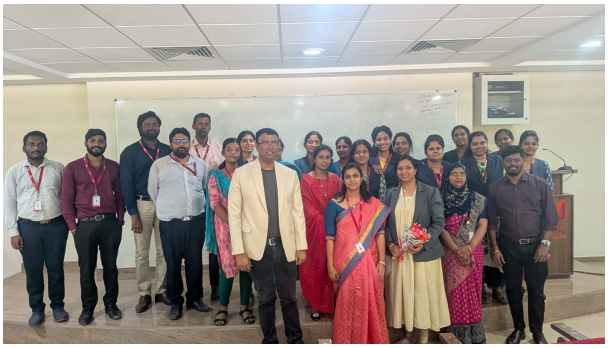

Figure 5: Group photo with resource persons Dr. Shushrutha and Dr. Trupti Sagar along with faculty participants on Day 1 of the FDP on "Next Generation Communication and Computing: From Massive MIMO to AI Acceleration on FPGA"

Figure 6: Hands-on Workshop on AI for Wireless Communication Systems using MATLAB and Simulink conducted by CoreEL Technologies during Day 1 of the FDP on "Next Generation Communication and Computing: From Massive MIMO to AI Acceleration on FPGA"

The afternoon session on Day 1 was conducted by **CoreEL Technologies**, focusing on **Modeling of Communication Systems and AI for Wireless Communications** using MATLAB and Simulink. The session started at 2 pm and began with an overview of the **Communication Toolbox**, highlighting its capabilities for designing and analysing communication systems. Participants were introduced to **modeling and analysing communication systems in Simulink**, covering key modulation techniques such as **ASK, PSK, and QAM**. A detailed demonstration of **QPSK modulation and demodulation** was provided, showcasing how Simulink can be

used for simulation and performance analysis. The session further explored **wireless waveform generation** and **wireless system modeling**, enabling participants to understand the complete workflow from signal generation to system-level analysis. Practical demonstrations reinforced the theoretical concepts, providing participants with hands-on experience in building and analysing wireless communication models that are integrated with AI-driven approaches.

Figure 7: Participants and resource persons during the group photo after the Hands-on Workshop on AI for Wireless Communication Systems using MATLAB and Simulink, conducted by CoreEL Technologies as part of Day 1 of the FDP.

Day 2 session started at 10.00 am, and was led by **Mohammed Raheem**, focusing on heterogeneous SoC architectures and their critical role in modern computing. The discussion emphasised the need for heterogeneous architectures to handle complex AI/ML workloads beyond traditional CPUs. Components of heterogeneous SoCs, such as CPU, GPU, NPU, TPU, DSP, and FPGA, were explained, along with interconnects and memory elements like NoC and chiplet-based architectures. Power management techniques such as Dynamic Voltage and Frequency Scaling (DVFS) were discussed, along with challenges in executing AI/ML workloads on conventional architectures. High-performance interconnects for heterogeneous computing, including NoC, CXL, HBM integration, and chiplet-based designs, were explored in detail. Strategies for power efficiency and thermal management were presented, followed by case studies on NVIDIA GPUs, Google TPUs, AMD Instinct, and Intel Habana, with performance benchmarks and comparisons. The session concluded with future trends such as chiplets and 3D packaging, neuromorphic computing,

quantum-AI convergence, and AI-driven SoC design automation, along with industry adoption in real-world applications like data center acceleration, healthcare, and genomics.

Figure 8: Dr. Remashan, Professor from the ECE Department, presenting a bouquet to Mr. Mohammed Raheem as a gesture of appreciation during Day 2 of the FDP on Next Generation Communication and Computing.

Figure 9: Insightful session by Mohammed Raheem on heterogeneous SoC architectures and their role in accelerating AI/ML workloads, covering CPUs, GPUs, NPUs, TPUs, FPGAs, interconnects, power management, and future trends in chiplet-based and 3D packaging technologies.

The afternoon session of Day 2 was conducted at 2 pm by CoreEL Technologies. The session focused on "Introduction to AMD FPGA Architecture and Design Flow" and provided participants with an in-depth understanding of the complete FPGA development cycle. The resource person explained the AMD FPGA architecture, highlighting its advanced features and capabilities for high-performance computing and AI acceleration. The session covered the design creation flow, including source and block insertion mechanisms, followed by design elaboration and simulation using testbenches and data force mechanisms. Participants were introduced to synthesis and implementation processes, along with techniques for I/O constraining, analysing resource utilisation, and identifying DRC (Design Rule Check) violations. The session also demonstrated bitstream generation and programming on hardware, enabling participants to gain practical exposure to deploying designs on FPGA platforms. This hands-on experience bridged the gap between theoretical concepts and real-world applications, equipping attendees with essential skills for FPGA-based system design. The session was highly interactive, with participants engaging in discussions and clarifying doubts related to FPGA workflows. Overall, the workshop provided a comprehensive overview of AMD FPGA design methodologies and practical implementation strategies, making it an invaluable learning experience for faculty and students alike.

Figure 10: Hands-on session on AMD FPGA Architecture and Design Flow by CoreEL Technologies during Day 2 of the FDP.

The second day's afternoon session was dedicated to **FPGA Design Acceleration using AMD Vivado**, conducted by CoreEL Technologies. The session provided a

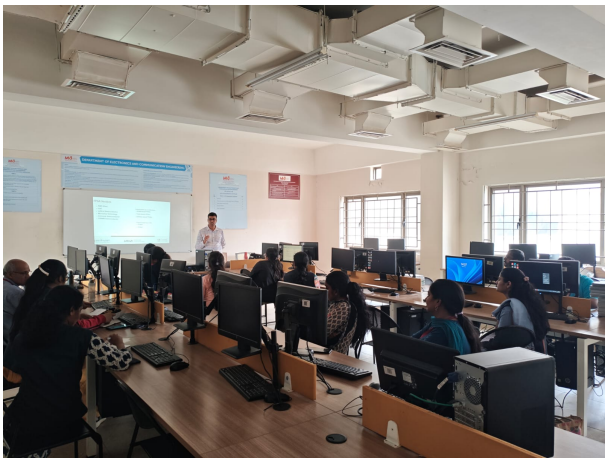

Figure 11: Interactive workshop on AMD FPGA Architecture and Design Flow conducted by CoreEL Technologies, empowering participants with practical skills in synthesis, simulation, and hardware programming during Day 2 of the FDP.

comprehensive introduction to **AMD FPGA architecture** and the **design creation flow**, including source and block insertion mechanisms. Participants learned about **design elaboration**, **simulation using testbench and data force mechanisms**, and the steps involved in **synthesis and implementation**. The session also covered **I/O constraining**, **resource utilisation analysis**, and handling **DRC (Design Rule Check) violations**. Finally, the process of **bitstream generation and programming on hardware** was demonstrated, giving participants practical exposure to deploying FPGA designs on real hardware platforms. This hands-on training equipped attendees with essential skills for accelerating AI and communication system designs using FPGA technology.

The third day of the Faculty Development Program started at 9.40 am and was featured by Dr. Ravi Shankar S, Professor at RVCE, focusing on the evolution of wireless communication systems from 2G to 6G and emerging technologies like ISAC (Integrated Sensing and Communication). The session began with an overview of the evolution to broadband rates in wireless systems, highlighting the transition from narrowband in early generations to high-speed broadband in 4G and beyond. Dr. Ravi Shankar explained the major entities in a communication system, providing a glimpse into the transmitter-receiver architecture across generations (2G through 6G) and the role of the wireless channel.

Figure 12: Group photo captured during Day 2 of the 3-Day Faculty Development Program on "Next Generation Communication and Computing: From Massive MIMO to AI Acceleration on FPGA", featuring participants, resource persons, and organisers.

Figure 13: Dr. Thilagraj, Head of IIoT Department, presenting a bouquet to Dr. Ravi Shankar S, Professor at RVCE, as a gesture of appreciation during Day 3 of the FDP on "Next Generation Communication and Computing".

Key topics covered included:

Communication requirements and needs driving the evolution from 2G to 3G,4G,5G,6G. Modulation techniques and over-the-air interfaces, mapping 4G and 5G standards to typical hardware platforms. 6G advancements, including the extraction of location parameters, range, and velocity of communicating devices. Modem architecture blocks: Bit processing, symbol processing, and RF processing. Multicarrier Modulation (MCM) and DMT transceiver architecture, along with RF blocks from 1G to 6G. Delay spread and multipath fading in wireless channels and their impact on system design. Wireless value chain and importance of standards, including IMT and LTE service classes. 5G use cases, separation of signaling and transport, and evolution in LTE architecture. User Equipment functional elements and challenges in wireless transmission mediums. Satellite communication systems and their integration with terrestrial networks.

Figure 14: Dr. Ravi Shankar S, Professor at RVCE, delivering an insightful lecture on the evolution of wireless communication systems during Day 3 of the FDP on "Next Generation Communication and Computing"

The session also delved into Shannon's Information Capacity Law and its modified versions, illustrating with a simple design example. Dr. Ravi Shankar provided historical context on ADSS standards, discussed types of multicarrier modulation, support algorithms, and challenges such as Peak-to-Average Power Ratio (PAPR). The lecture concluded with future trends in wireless communication, emphasising 6G capabilities, ISAC integration, and advanced RF architectures, along with practical consider-

ations for real-world deployment. This comprehensive session offered participants a deep understanding of the technological evolution, design challenges, and future directions in wireless communication systems, making it a highly valuable learning experience. The afternoon session of Day 3 was conducted by Mr. Vishnu, Senior Application Engineer from CoreEL Technologies. The session focused on advanced FPGA design techniques and embedded system development. The topics delivered included:

Hardware Debug using ILA and VIO: Mr. Vishnu explained the use of Integrated Logic Analyzer (ILA) and Virtual Input/Output (VIO) for real-time debugging of FPGA designs. Participants learned how these tools help in monitoring internal signals and validating design functionality without external hardware probes.

Embedded Design Flow: The session covered the complete embedded design workflow, from hardware platform creation to software integration, emphasising the importance of efficient design partitioning and resource utilisation. Introduction to MicroBlaze Architecture: A detailed overview of MicroBlaze, the soft processor core for Xilinx FPGAs, was provided. The discussion included its architecture, instruction set, and applications in embedded systems. AXI Peripheral-Based Design: Participants were introduced to AXI (Advanced eXtensible Interface) protocol and its role in connecting peripherals within FPGA-based systems. The session demonstrated how AXI facilitates high-speed communication between IP blocks and accelerators.

The workshop was highly interactive, with hands-on demonstrations that allowed participants to implement debugging techniques, configure MicroBlaze processors, and integrate AXI peripherals in a design environment. This practical exposure enhanced their understanding of embedded FPGA workflows and real-world applications.

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Outcomes and Impact

- Enhanced understanding of advanced wireless communication technologies, including Massive MIMO, intelligent surfaces, and beamforming.
- Practical exposure to AI-driven wireless communication systems using MAT-

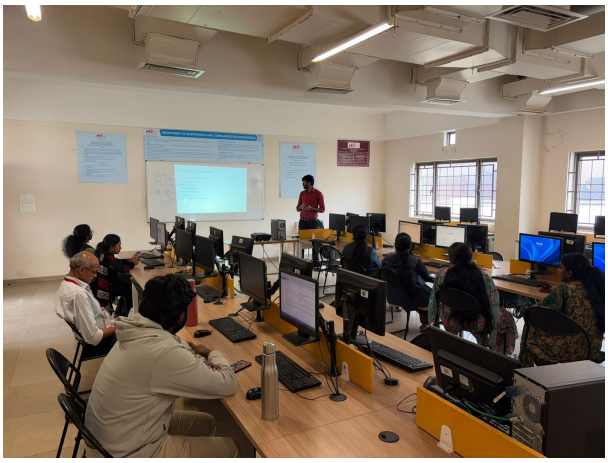

Figure 15: Participants engaged in a hands-on session on FPGA debugging and embedded design flow, conducted by Mr. Vishnu from CoreEL Technologies during Day 3 of the FDP

LAB and Simulink.

- Hands-on experience in FPGA-based design and implementation using Xilinx Vivado and Nexys A7 boards.
- Insights into antenna design, simulation, and fabrication for modern wireless applications.
- Identification of emerging research areas such as AI acceleration, RIS channel modeling, and FPGA-based optimization.

Impact: The three-day Faculty Development Program had a significant impact on participants by enhancing their knowledge and skills in next-generation communication and computing technologies. Faculty members gained:

- **Advanced Technical Knowledge**: Deep understanding of Massive MIMO, beamforming, intelligent surfaces, and heterogeneous SoC architectures.
- **Hands-on Expertise**: Practical experience with MATLAB, Simulink, Xilinx Vivado, and FPGA-based design, bridging theory and real-world applications.

- **Research Orientation**: Exposure to emerging research areas such as RIS channel modeling, AI-driven MIMO control, and FPGA acceleration for AI workloads.
- **Industry Readiness**: Insights into cutting-edge technologies adopted by leading companies (NVIDIA, Google, AMD, Intel), preparing faculty to guide students toward industry-relevant projects.
- **Collaborative Learning**: Interaction with experts from academia and industry fostered networking and potential collaborations for future research and development.

This FDP empowered faculty to integrate advanced concepts into curriculum design, mentor students on innovative projects, and contribute to research aligned with global technological trends.

Figure 16: Group photo marking the successful conclusion of the 3-Day Faculty Development Program on "Next Generation Communication and Computing: From Massive MIMO to AI Acceleration on FPGA", with participants, resource persons, and organisers.

Conclusions

The three-day FDP successfully achieved its objectives by combining theoretical knowledge with practical training. It provided participants with a holistic view of next-generation communication and computing technologies, preparing them to

contribute to cutting-edge research and industry applications. The sessions facilitated knowledge sharing among experts and participants, fostering collaboration and innovation in the field of electronics and communication engineering.

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