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Department of Electronics Engineering (VLSI Design and Technology)

Report on the Guest lecture on "RTL to GDS Flow in Industry"

The department of **Electronics Engineering (VLSI Design and Technology)** conducted a **Guest Lecture** titled **"RTL to GDS Flow in Industry"** on **25-05-2026** from **10:00 AM to 12:30 PM**, in **Seminar Hall 2**.

Objectives of the Event

The primary objectives of the event are:

- To introduce students to the complete RTL to GDSII design flow used in the semiconductor industry.
- To provide understanding of major VLSI physical design stages such as synthesis, floor planning, placement, CTS, routing, and verification.
- To familiarize students with industry-standard EDA tools and timing analysis concepts used in modern chip design.
- To bridge the gap between theoretical VLSI concepts and practical industrial implementation.
- To provide exposure to career opportunities and real-time workflows in the semiconductor and VLSI domain.

Event Overview

The Guest Lecture on "RTL to GDS Flow in Industry" was delivered by Mr. Rahul Vishal, Senior Director – Physical Design at Radiant Semiconductors, who has 25 years of experience in VLSI design. The resource person has worked at Intel Corporation, Texas instruments, NXP semiconductors and Bharat Electronics. With extensive industrial experience in physical design and semiconductor implementation, the speaker shared valuable insights into real-world VLSI chip design methodologies and industry practices. During the session, the speaker explained the complete

RTL-to-GDSII flow, which describes how the RTL code is translated into a manufacturable chip layout. The lecture began with an introduction to RTL design and logic synthesis, where RTL descriptions are converted into gate-level netlists using synthesis tools such as Synopsys Design Compiler and Cadence Genus.

The session was attended by VLSI students and faculty members, offering them valuable insights into the industrial aspects of the RTL-to-GDSII design flow. Mr. Rahul Vishal's industry-oriented perspective helped participants understand how theoretical VLSI concepts are applied in real-time semiconductor design workflows, providing valuable insights into modern chip design, physical design implementation, and industry practices in advanced electronics manufacturing.

0.1 Guest Lecture session

Day	Time	Session Details
Monday, May 25 2026	10.00 - 10.10 am 10.10am - 12.30 pm	Welcome Address & Introduction of Guest Guest Lecture

Table 1: Schedule of the Event

Welcome Address

Figure 1 shows Nimishasri, a first-year, M.Tech student, presenting the welcome address.

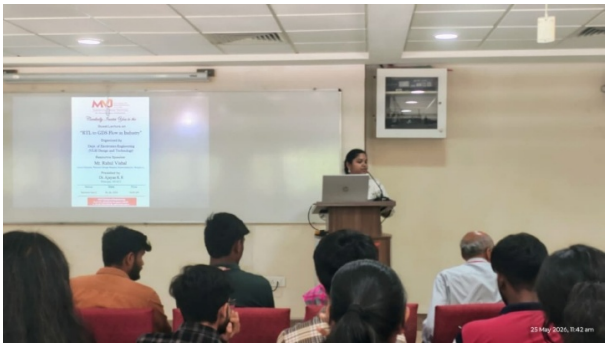
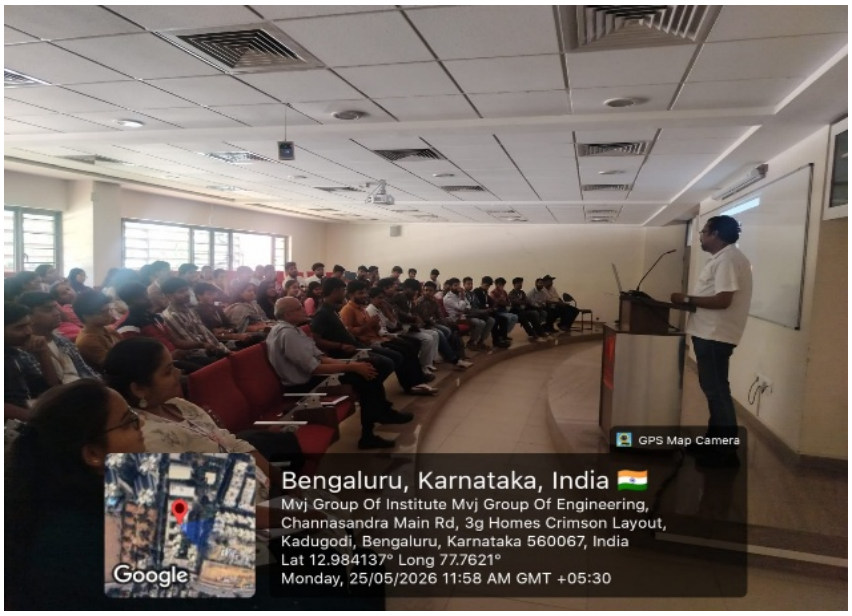


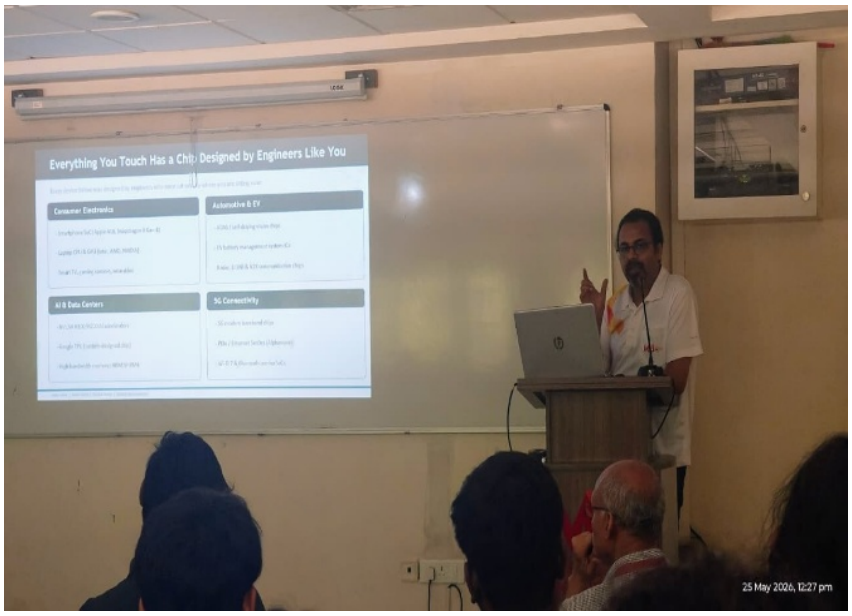
Figure 1: Welcome Address by Nimishasri

Figure 2 shows the picture of students and faculties attending the session (2a) and

Mr. Rahul Vishal, the resource person delivering the lecture (2b).



(a) Students and faculty members attending the lecture by Mr. Rahul Vishal.



(b) Mr. Rahul Vishal, delivering the lecture

Figure 2

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Event Overview

The speaker described the role of SDC (Synopsys Design Constraints) in defining timing requirements and explained key timing parameters, including Setup Time, Hold Time, Worst Negative Slack (WNS), and Total Negative Slack (TNS). The speaker also explained the concepts of timing closure and optimization for performance, area, and power in detail.

The session further covered the different phases of synthesis which included elaboration, Technology by mapping and optimization techniques. The speaker explained how abstract RTL logic is mapped to standard-cell libraries and optimized for timing and power constraints.

The lecture also focused on the Physical Design Flow, in which the synthesized netlist is converted into a physical chip layout. The important stages in a physical design are: Floor planning, Power planning, Placement, Clock tree synthesis (CTS), Routing, Verification and sign-off. Detailed explanation was provided on placement techniques such as global placement, detailed placement, congestion-driven optimization, and timing-driven placement. The importance of minimizing wire delay and achieving timing closure was highlighted.

The speaker also explained Physical Verification processes including: DRC (Design rule check) and LVS (Layout versus schematic) which ensure that the layout satisfies fabrication rules and correctly matches the intended circuit design.

The speaker also discussed the concept of PVT (Process, Voltage, and Temperature) variations and their impact on chip performance and timing analysis . The session concluded with insights into tape-out procedures and the generation of final GDSII files sent to semiconductor foundries for fabrication.

The lecture provided students with a clear understanding of industrial VLSI workflows and exposed them to the practical challenges encountered in semiconductor chip design and implementation.

The guest lecture concluded with an engaging interactive session in which students and faculty members clarified their doubts regarding the RTL to GDSII flow, timing closure, physical verification and industrial design practices.

Outcomes and Impact

- Enhanced Understanding of RTL to GDS Flow – Students gained a comprehensive understanding of the complete semiconductor design flow from RTL coding to final GDSII generation.

- Exposure to Industry Tools and Practices – The lecture introduced students to industry-standard EDA tools such as Synopsys and Cadence used in VLSI design companies.

- Understanding of Timing Analysis – Participants learned important timing concepts such as setup time, hold time, WNS, and TNS, along with timing optimization techniques.

- Knowledge of Physical Design Stages – Students developed practical understanding of floor planning, placement, CTS, routing, and physical verification processes.

Conclusions

The guest lecture on "RTL to GDS Flow in Industry" provided a valuable platform for participants to enhance their knowledge in chip design. The active engagement of the participants demonstrated their keen interest in learning practical challenges in VLSI chip design.

Report by: Assistant Prof. M Poornima

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