Affiliated to VTU, Belagavi

Approved by AICTE, New Delhi

Recognized by UGC under 2(f) & 12 (B)

Department of Electronics Engineering (VLSI Design and Technology)

Report on the Add-on Lecture "Low-Power IC Design"

The Department of **Electronics Engineering (VLSI Design and Technology)** conducted an **Add-on Lecture** titled **"Low-Power IC Design"** on **31-08-2026** from **10:00 AM to 12:30 PM** in **Seminar Hall 1**.

Objectives of the Event

The primary objectives of the event were:

- To introduce students to the fundamentals of power consumption in digital circuits and explain why low-power IC design is critical in modern VLSI systems.
- To provide an understanding of the factors affecting power consumption, namely dynamic power (switching and short-circuit power) and static power (leakage power).
- To familiarize students with industry-standard low-power design techniques such as clock gating, power gating, multi-voltage design, and Dynamic Voltage and Frequency Scaling (DVFS).
- To bridge the gap between theoretical VLSI concepts and the practical industrial implementation of power-performance trade-offs.
- To expose students to real-world reliability challenges such as voltage droop and thermal throttling, along with the mitigation techniques used in the semiconductor industry.

Event Overview

The Add-on Lecture on **"Low-Power IC Design"** was delivered by **Mr. Srinivas B. P., Manager (GPU Division), Intel Corporation, Bengaluru**. The resource person has previously worked at **International Business Machines (IBM) Corporation, Infineon Technologies, and Bharat Electronics Limited (BEL)**. With extensive industry experience in GPU design and low-power semiconductor implementation, Mr. Srinivas shared valuable insights into real-world power management methodologies followed in the semiconductor industry. The session covered a broad spectrum of topics, ranging from fundamental power equations to advanced voltage droop mitigation architectures used in modern production processors.

During the session, the speaker provided a comprehensive overview of power consumption in digital circuit design and highlighted why low-power design has become a critical and indispensable aspect of modern chip development. He discussed the various components contributing to power consumption, key low-power design challenges, and major industry-adopted techniques, including transistor selection, clock gating, power gating, state retention during power gating, multi-voltage design with level shifters, DVFS, and Unified Power Format (UPF)-based design and verification.

The session was attended by students and faculty members from the Departments of **Electronics Engineering (VLSI Design and Technology)** and **Electronics and Communication Engineering**. The speaker's industry-oriented perspective enabled participants to understand how theoretical VLSI concepts are translated into practical power, performance, and thermal management solutions employed in modern processors.

Outcome of the Event

The lecture enhanced participants' understanding of low-power IC design methodologies and their significance in contemporary semiconductor systems. Students gained valuable insights into industry practices, power optimization strategies, and real-world design challenges, thereby strengthening their knowledge of VLSI design concepts and their practical applications in advanced processor development.

Figure 1: Welcome address by Maria, 7th semester student, Department of Electronics Engineering (VLSI Design and Technology)

Figure 2: Dr. Remashan Kariyadan, HoD, Department of Electronics Engineering (VLSI Design and Technology) welcoming Srinivas B P, the resource person, with a floral bouquet

Add-on Lecture session

Day	Time	Session Details
Monday, August 31 2026	10.00 - 10.10 am	Welcome Address
	10.10 - 12.30 pm	Add-on Lecture

Table 1: Schedule of the Event

Figure 3: Mr. Srinivas B P delivering the lecture on Low-Power IC Design

Figure 4: Students attending the Add-on Lecture

Outcomes and Impact

- **Enhanced Understanding of Low-Power Design:** Participants gained a clear understanding of the power, performance, and thermal trade-offs involved in modern VLSI chip design.
- **Exposure to Industry Practices:** The session provided valuable insights into industry-standard low-power design techniques, including clock gating, power gating, Dynamic Voltage and Frequency Scaling (DVFS), multi-voltage design, and UPF-based design verification widely adopted in semiconductor industries.
- **Understanding of Reliability Engineering:** Students learned about critical reliability challenges such as voltage droop, thermal throttling, and guard-banding, along with industry-adopted mitigation strategies including adaptive clocking and instruction throttling.
- **Bridging Theory and Practice:** The lecture enabled students to correlate theoretical VLSI concepts with real-world industrial implementations through practical case studies, including CPM-based slope detection techniques used in production processors.
- **Industry-Oriented Learning:** Interactions with an experienced industry professional provided students with a deeper understanding of current trends, challenges, and best practices in low-power semiconductor design.
- **Improved Awareness of Advanced Processor Design:** Participants gained exposure to the power management methodologies employed in modern GPUs and processors, enhancing their understanding of contemporary semiconductor technologies.

Conclusion

The Add-on Lecture on **“Low-Power IC Design”** provided a valuable platform for

participants to enhance their knowledge of low-power IC design techniques, thermal management, and industry-oriented design practices. The session offered significant insights into contemporary challenges and solutions in semiconductor design, enabling participants to better understand the power, performance, and reliability considerations involved in modern VLSI systems. The active engagement and enthusiastic participation of the attendees reflected their keen interest in learning about the practical aspects and real-world challenges of low-power IC design. Overall, the lecture successfully bridged the gap between academic concepts and industrial applications, enriching the learning experience of both students and faculty members.

Report by: Assistant Prof. Ankita Kumari

Affiliation: Faculty in the Department of Electronics Engineering (VLSI Design and Technology)

MVJ College of Engineering