



Bachelor of Engineering

in

Electronics Engineering
(VLSI Design and Technology)

Scheme and Syllabus
(2025 Scheme & 3rd Semester Syllabus)



VISION OF THE INSTITUTE

Be an Institution of Excellence with International Standards.

MISSION OF THE INSTITUTE

- Impart quality education, along with industrial exposure
- Provide world-class facilities to undertake research activities relevant to industrial and professional needs.
- Promote Innovation, Entrepreneurship and Value-added education that is socially relevant, along with economic benefits.

VISION OF THE DEPARTMENT

- Imparting quality technical education through interdisciplinary research, innovation and progressive learning, for developing sustainable technology in the area of VLSI and Embedded Systems.

MISSION OF THE DEPARTMENT

- **Professional Growth:** Deliver technically sound education to produce industry-ready engineers with a strong inclination toward research and innovation.
- **Skill Development:** Equip students with future-focused skills and instil a drive to explore modern and emerging technologies.
- **Research Culture:** Establish Centres of Excellence in VLSI and Embedded Systems through strategic industry and academic collaborations.
- **Employment & Entrepreneurship:** Foster an entrepreneurial mindset and innovation to promote self-employment and job creation in the tech ecosystem.

PROGRAM OUTCOMES:

1. **Engineering Knowledge:** Apply knowledge of mathematics, natural science, computing, engineering fundamentals and an engineering specialization as specified in WK1 to WK4 respectively to develop to the solution of complex engineering problems.
2. **Problem Analysis:** Identify, formulate, review research literature and analyze complex engineering problems reaching substantiated conclusions with consideration for sustainable development.
3. **Design/Development of Solutions:** Design creative solutions for complex engineering problems and design/develop systems/components/processes to meet identified needs with consideration for the public health and safety, whole-life cost, net zero carbon, culture, society and environment as required.
4. **Conduct Investigations of Complex Problems:** Conduct investigations of complex engineering problems using research-based knowledge including design of experiments, modelling, analysis & interpretation of data to provide valid conclusions.
5. **Engineering Tool Usage:** Create, select and apply appropriate techniques, resources and modern engineering & IT tools, including prediction and modelling recognizing their limitations to solve complex engineering problems.
6. **The Engineer and The World:** Analyze and evaluate societal and environmental aspects while solving complex engineering problems for its impact on sustainability with reference to economy, health, safety, legal framework, culture and environment.
7. **Ethics:** Apply ethical principles and commit to professional ethics, human values, diversity and inclusion; adhere to national & international laws.
8. **Individual and Collaborative Teamwork:** Function effectively as an individual, and as a member or leader in diverse/multi-disciplinary teams.
9. **Communication:** Communicate effectively and inclusively within the engineering community and society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations considering cultural, language, and learning differences.
10. **Project Management and Finance:** Apply knowledge and understanding of engineering management principles and economic decision-making and apply these to one's own work, as a member and leader in a team, and to manage projects and in multidisciplinary environments.

11. **Life-Long Learning:** Recognize the need for and have the preparation and ability for i) independent and life-long learning ii) adaptability to new and emerging technologies and iii) critical thinking in the broadest context of technological change.

PROGRAM EDUCATIONAL OBJECTIVES (PEOS):

- **Professional Development:** Graduates will have successful careers in various domains of VLSI design in associated industries or higher education and research.
- **Attitude towards Lifelong Learning:** Graduates will have the ability and attitude to adapt to evolving technological changes and challenges.
- **Innovative Research:** To include group work and team management skills to promote knowledge transfer, leading to conceptualisation and delivery of real-time industry and society-related projects with various complexities.

PROGRAM SPECIFIC OUTCOMES (PSOS):

- **Design proficiency:** To design various methodologies in aspects of digital and analog VLSI circuits with reference to ASIC (full-custom, Semi-Custom) and FPGA.
- **Core Skill Sets:** To gain proficiency in using industry-standard Electronic Design Automation (EDA) tools such as CADENCE and AMD-Xilinx for the development of chips, including CMOS-ICs, IPs, and SoCs. They will also acquire the skills necessary to conduct pre- and post-silicon validation/testing by developing automated frameworks using Python and TCL

MVJ College of Engineering, Bengaluru (Autonomous)
B.E. in Electronics Engineering (VLSI Design and Technology) - Scheme 2025
 Outcome-Based Education (OBE) and Choice-Based Credit System (CBCS)
 (Applicable for 2025-26 admitted students)

Semester - III

Sl. No	Course	Course Code	Course Title	Teaching & Learning Scheme					Examination				Credits
				CI		LI	TW & SL	# TH / S	Duration in h ours	CIE Marks	SEE Marks	Total Marks	
1	ASC	MVJ25EC31	Probability and Transformation Techniques	56	0	0	64	120	3	50	50	100	4
2	IPCC	MVJ25VL32	Computer organization and architecture	42	0	28	50	120	3	50	50	100	4
3	PCC	MVJ25VL33	Analog Electronics	56	0	0	64	120	3	50	50	100	4
4	PCC	MVJ25EC34	Network Analysis	56	0	0	64	120	3	50	50	100	4
5	PCC	MVJ25VL35	Analysis and Design of Digital circuits	42	0	0	48	90	3	50	50	100	3
6	PCCL	MVJ25VLL36	Digital Circuit Laboratory	0	0	28	2	30	3	50	50	100	1
7	AEC	MVJ25AECK37	Sustainable engineering and SDGs	14	0	0	16	30	2	50	50	100	1
8	SDC	MVJ25EC38SL	LabVIEW for ECE	0	0	28	2	30	3	50	50	100	1
9	NCMC	MVJ25PE39	Physical Education (PE) (Sports and Athletics)	0	0	0	28	28	---	100	---	100	PP
		MVJ25YO39	Yoga										
10	NCMC	MVJ25MATDIP310	Additional Mathematics – I *	42	0	0	0	48	—	100	---	100	PP
TOTAL													22

*Applicable for Lateral entry students only

MVJ College of Engineering, Bengaluru (Autonomous)
B.E. in Electronics Engineering (VLSI Design and Technology) - Scheme 2025
Outcome-Based Education (OBE) and Choice-Based Credit System (CBCS)
(Applicable for 2025-26 admitted students)

Semester - IV

Sl. No	Course	Course Code	Course Title	Teaching & Learning Scheme					Examination				Credits
				CI		LI	TW & SL	# TH / S	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	SL						
1	PCC	MVJ25VL41	Control Systems	56	0	0	64	120	3	50	50	100	4
2	IPCC	MVJ25VL42	VLSI Design flow: RTL to GDS - I	42	0	28	50	120	3	50	50	100	4
3	PCC	MVJ25VL43	Advanced Computer organization and architecture	56	0	0	64	120	3	50	50	100	4
4	PCC	MVJ25VL44	Signals and Systems	56	0	0	64	120	3	50	50	100	4
5	PCCL	MVJ25VLL45	Signals and Systems Laboratory	0	0	28	2	30	3	50	50	100	1
6	BSC	MVJ25BI46	Biology for Engineers	28	0	0	32	60	3	50	50	100	2
7	AEC	MVJ25AECK47	Scientific Foundation of Health	0	0	28	2	30	3	50	50	100	1
8	SDL	MVJ25EC48SL	Semiconductor Devices simulation lab	0	0	28	2	30	3	50	50	100	1
9	NCCMC	MVJ25PE49	Physical Education (PE) (Sports and Athletics)	0	0	0	28	28	---	100	---	100	PP
		MVJ25YO49	Yoga										
10	NCCMC	MVJ25MATDIP410	Additional Mathematics – II *	42	0	0	0	48	---	100	---	100	PP
TOTAL													21

Sl. No	Course	Course Code	Course Title	Teaching & Learning Scheme					Examination				Credits
				CI		LI	TW & SL	# TH / S	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	SL						
1	HSMC	MVJ25VL51	Engineering Economics and Management	42	0	0	48	90	3	50	50	100	3
2	IPCC	MVJ25VL52	VLSI Design flow: RTL to GDS - II	42	0	28	50	120	3	50	50	100	4
3	PCC	MVJ25VL53	Digital VLSI Design	42	0	0	48	90	3	50	50	100	3
4	PCC	MVJ25VL54	Engineering Electromagnetics	42	0	0	48	90	3	50	50	100	3
5	PEC	MVJ25VL55X	Professional Elective Course-I	42	0	0	48	90	3	50	50	100	3
6	BSC	MVJ25RM56	Research Methodology and IPR (Online)	28	0	0	32	60	3	50	50	100	2
7	AEC	MVJ25AECK57	Ability Enhancement Course	14	0	0	16	30	2	50	50	100	1
8	SDC	MVJ25EC58SL	MATLAB and Simulink programming and modelling	0	0	28	2	30	3	50	50	100	1
9	PCCL	MVJ25VLL59	Digital VLSI Design Laboratory	0	0	28	2	30	3	50	50	100	1
10	SDC	MVJ25HBP510	Hackathon-Based Project	42	0	0	0	48	---	100	---	100	PP
1	HSMC	MVJ25VL51	Engineering Economics and Management	42	0	0	0	48	---	100	---	100	PP
TOTAL													23
Professional Elective Course-I													
MVJ25VL55A		Machine Learning		MVJ25VL55C		Design for testability							
MVJ25VL55B		Linux and scripting languages		MVJ25VL55D		RF and Quantum Computing							

MVJ College of Engineering, Bengaluru (Autonomous)
B.E. in Electronics Engineering (VLSI Design and Technology) - Scheme 2025
 Outcome-Based Education (OBE) and Choice-Based Credit System (CBCS)
 (Applicable for 2025-26 admitted students)

Semester - VI

Sl. No	Course	Course Code	Course Title	Teaching & Learning Scheme					Examination				Credits
				CI		LI	TW & SL	# TH / S	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	IPCC	MVJ25VL61	System Verilog	42	0	28	50	120	3	50	50	100	4
2	PCC	MVJ25VL62	Embedded systems	42	0	0	48	90	3	50	50	100	3
3	PCC	MVJ25VL63	SoC design	42	0	0	48	90	3	50	50	100	3
4	PCC	MVJ25VL64	Analog VLSI and Mixed Digital Circuit Design	42	0	0	48	90	3	50	50	100	3
5	PEC	MVJ25VL65X	Professional Elective Courses-II	42	0	0	48	90	3	50	50	100	3
6	PCCL	MVJ25VLL66	Analog VLSI Laboratory	0	0	28	2	30	3	50	50	100	1
7	AEC	MVJ25AECK67	Ability Enhancement Course	0	0	28	2	30	3	50	50	100	1
8	SDC	MVJ25EC68SL	AI for Communication Systems	0	0	28	2	30	3	50	50	100	1
9	SDC	MVJ25VL69	Capstone Project – Phase 1	42	0	0	48	90	3	50	50	100	3
10	NCMC	MVJ25UHV610	Universal Human Values	42	0	0	0	48	---	100	---	100	PP
TOTAL													22

MVJ25VL65A	Artificial Intelligence for IC design	MVJ25VL65C	High power VLSI Design
MVJ25VL65B	Memory Devices	MVJ25VL65D	Static timing analysis and signoff

MVJ College of Engineering, Bengaluru (Autonomous)
B.E. in Electronics Engineering (VLSI Design and Technology) - Scheme 2025
Outcome-Based Education (OBE) and Choice-Based Credit System (CBCS)
(Applicable for 2025-26 admitted students)

Semester – VII (Swappable VII and VIII SEMESTER) (SCHEME-A)

Sl. No	Course	Course Code	Course Title	Teaching & Learning Scheme					Examination				Credits
				CI		LI	T ^W	# TH / S	Duration	CIE Marks	SEE Marks	Total Marks	
				L	T	P	SL						
1	IPCC	MVJ25VL71	Universal Verification Methodology	42	0	28	50	120	3	50	50	100	4
2	PEC	MVJ25VL72X	Professional Elective Course-III	42	0	0	48	90	3	50	50	100	3
3	PEC	MVJ25VL73X	Professional Elective Course -IV	42	0	0	48	90	3	50	50	100	3
4	OEC	MVJ25xx74X	Open Elective Course-I	42	0	0	48	90	3	50	50	100	3
5	SDC	MVJ25VL75	Capstone Project - Phase-II	-	-	-	-	-	-	50	50	100	7
6	NCMC	MVJ25IKS76	Indian Knowledge System	42	0	0	0	48	---	100	---	100	PP
7	AEC	MVJ25AECK77	Ability Enhancement Course	0	0	28	2	30	3	50	50	100	1
8	SDC	MVJ25EC78SL	Design Flow for VLSI Chips	0	0	28	2	30	3	50	50	100	1
TOTAL													22
Professional Elective Course-III													
MVJ25VL72A		Nano electronic devices		MVJ25VL72C		VLSI Interconnects							
MVJ25VL72B		VLSI Digital Signal Processing											
Professional Elective Course-IV													
MVJ25VL73A		Hardware Security		MVJ25VL73C		Compound Semiconductor Devices							
MVJ25VL73B		Bio-Medical CMOS ICs		MVJ25VL73D		VLSI for automotive industry							
Open Elective Course-I													
MVJ25VL74A		Introduction to VLSI Design flow		MVJ25EVL4C		Semiconductor Industry and its global impacts							
MVJ25VL74B		Introduction to VLSI Fabrication		MVJ25XX74D		Foreign Language (NPTEL/SWAYAM/online VTU)							

MVJ College of Engineering, Bengaluru (Autonomous)
B.E. in Electronics Engineering (VLSI Design and Technology) - Scheme 2025
 Outcome-Based Education (OBE) and Choice-Based Credit System (CBCS)
 (Applicable for 2025-26 admitted students)

Semester – VIII (Swappable VII and VIII SEMESTER) (SCHEME-A)

Sl. No	Course	Course Code	Course Title	Teaching & Learning Scheme					Examination				Credits
				CI		LI	TW & SL	# TH / S	Duration in h ours	CIE Marks	SEE Marks	Total Marks	
1	PEC	MVJ25VL81X	Professional Elective-V (NPTEL/VTU Online Course)	42	0	0	48	90	3	50	50	100	3
2	OEC	MVJ25VL82X	Open Elective-II (NPTEL/VTU Online Course)	42	0	0	48	90	3	50	50	100	3
3	SDC	MVJ25INT83X	Internship (15 weeks or 90 working days)	56	0	0	64	120	3	100	100	200	9
TOTAL													15

MVJ25VL81A	NPTEL/VTU Online Course	MVJ25VL81C	NPTEL/VTU Online Course
MVJ25VL81B	NPTEL/VTU Online Course	MVJ25VL81D	NPTEL/VTU Online Course
Open Elective-II			
MVJ25VL82A	NPTEL/VTU Online Course	MVJ25VL82C	NPTEL/VTU Online Course
MVJ25VL82B	NPTEL/VTU Online Course	MVJ25VL82D	NPTEL/VTU Online Course

Types of Internships (Course Code: MVJ25INT83X)

Students shall undertake one of the following internship types during the eighth semester, as per academic guidelines:

- MVJ25INT83A – Industry Internship:** Shall involve practical exposure and training within an industrial or corporate setting.
- MVJ25INT83B – Research Internship:** Shall focus on academic or applied research under the guidance of faculty or research institutions.
- MVJ25INT83C – Post-Placement Internship:** Shall be undertaken by students who have secured placement, aligning with their future employment domain.
- MVJ25INT83D – Societal Internship:** Shall engage students in community-based or social impact projects with NGOs, government bodies, or civic organizations.
- MVJ25INT83E – Online Internship:** Shall be conducted through recognized digital platforms offering structured internship modules.
- MVJ25INT83F – Skill Enhancement Internship:** Shall be opted by students unable to secure internships, offering credit equivalence through curated online courses available at <http://www.online.vtu.ac.in>

Professional Elective Course-III			
MVJ25VL72A	NPTEL/VTU Online Course	MVJ25VL72C	NPTEL/VTU Online Course
MVJ25VL72B	NPTEL/VTU Online Course	MVJ25VL72D	NPTEL/VTU Online Course
Professional Elective Course-IV			
MVJ25VL73A	NPTEL/VTU Online Course	MVJ25VL73C	NPTEL/VTU Online Course
MVJ25VL73B	NPTEL/VTU Online Course	MVJ25VL73D	NPTEL/VTU Online Course
Open Elective Course-I			
MVJ25VL74A	NPTEL/VTU Online Course	MVJ25VL74C	NPTEL/VTU Online Course
MVJ25VL74B	NPTEL/VTU Online Course	MVJ25VL74D	NPTEL/VTU Online Course
Professional Elective Course-V			
MVJ25VL81A	NPTEL/VTU Online Course	MVJ25VL81C	NPTEL/VTU Online Course
MVJ25VL81B	NPTEL/VTU Online Course	MVJ25VL81D	NPTEL/VTU Online Course
Open Elective Course-II			
MVJ25VL82A	NPTEL/VTU Online Course	MVJ25VL82C	NPTEL/VTU Online Course
MVJ25VL82B	NPTEL/VTU Online Course	MVJ25VL82D	NPTEL/VTU Online Course

Types of Internships (Course Code: MVJ25INT83X)

Students shall undertake one of the following internship types during the eighth semester, as per academic guidelines:

1. **MVJ25INT83A – Industry Internship:** Shall involve practical exposure and training within an industrial or corporate setting.
2. **MVJ25INT83B – Research Internship:** Shall focus on academic or applied research under the guidance of faculty or research institutions.
3. **MVJ25INT83C – Post-Placement Internship:** Shall be undertaken by students who have secured placement, aligning with their future employment domain.
4. **MVJ25INT83D – Societal Internship:** Shall engage students in community-based or social impact projects with NGOs, government bodies, or civic organizations.
5. **MVJ25INT83E – Online Internship:** Shall be conducted through recognized digital platforms offering structured internship modules.
6. **MVJ25INT83F – Skill Enhancement Courses (SEC):** Shall be opted by students unable to secure internships, offering credit equivalence through curated online courses available at [http:// www.online.vtu.ac.in](http://www.online.vtu.ac.in)

To ensure uniformity, quality, and transparency in the internship process, **VTU has launched a centralized web portal** that serves as a **single platform** for all internships opportunities. Reputed **industries, Centers of Excellence, Research Laboratories**, and other recognized bodies will be registered on this portal. **Students must choose internships exclusively through this portal. No other mode of internship selection will be permitted.**

B.E, III Semester, Electronics Engineering (VLSI design and Technology)

Probability and Transformation techniques			
Course Code	MVJ25EC31	Scheme	2025
Type of course	ASC	Semester	III
Teaching hours / week (L: T:P)	4:0:0	CIE Marks	50
Total Hours of Pedagogy (L: T:P:SL & TW)	56:0:0:64	SEE Marks	50
Credits	4	Total	100
Examination type (SEE)	Theory	Exam hours	3
Course Objectives: This course will give ability to: • Apply discrete and continuous probability distributions in analysing the probability models arising in engineering field. • Understand the concepts of Complex variables and transformation for solving Engineering Problems. • Demonstrate and present data using statistical method and fit the best curve for the data.			
Syllabus			
This course equips students with the ability to apply Discrete and continuous probability distributions to analyse engineering systems, signal behaviour, and data-driven models. It strengthens their understanding of complex variables and transformations, enabling effective problem-solving in areas such as communication systems, circuit design, and embedded technologies. Additionally, it develops skills in statistical analysis, data interpretation, and curve fitting, which are essential for performance evaluation, optimization, and decision-making in modern electronic and IoT-based applications.			
Course Plan			
Module I			
Probability Theory			
S. No	Topics to be covered		Hours required
1	Random variables for discrete and continuous time functions.		12
2	probability density function.		
3	Cumulative density function.		
4	Probability Distributions: Binomial distribution.		
5	Poisson distribution. Normal distribution, Exponential distribution.		
6	Joint probability distributions.		
Module II			

Complex Variables		
S. No	Topics to be covered	Hours required
1	Functions of complex variables, Analytic function, Properties of analytic functions.	11
2	Cauchy-Riemann equations in Cartesian form and polar coordinates.	
3	Construction of analytic function by using Milne-Thomson method.	
4	Transformations: Bi-linear Transformation, Conformal Transformation.	
5	Discussion of the transformations: $w = z^2, w = e^z$ and $w = z + \frac{1}{z} (z \neq 0)$.	
Module III		
Fourier series		
S. No	Topics to be covered	Hours required
1	Definition of Periodic functions, Dirichlet's condition.	11
2	Fourier series of periodic functions of period 2π .	
3	Fourier series of periodic functions of arbitrary period $2c$.	
4	Half-range Fourier Sine and cosine series.	
5	Practical Harmonic Analysis and Problems.	
Module IV		
Fourier transforms and Z-transforms		
S. No	Topics to be covered	Hours required
1	Infinite Fourier transforms, Fourier sine and cosine transform.	11
2	Inverse Fourier cosine and sine transform.	
3	Definition of Z-transforms, standard z-transforms, Damping, and shifting rules.	
4	Inverse Z-transforms by the partial fraction method.	
5	Solving difference equations by using Inverse Z-transform.	
Module V		
Statistical and Sampling theory		
S. No	Topics to be covered	Hours required
1	Definition of Correlation, Regression coefficients.	11
2	Line of regression problems.	
3	Fitting of the curves in the form $y = ax + b$ by the method of least squares.	
4	Sampling, Sampling distributions, Standard error.	

5	Student's t-distribution.	
6	Chi-square distribution.	
Textbooks: 1. B.S. Grewal, "Higher Engineering Mathematics", Khanna Publishers, 43rd Edition, 2013. 2. G.B. Gururajachar, "Engineering Mathematics-III", Academic Excellent Series Publications, 2016.		
Reference Books: 1. Erwin Kreyszig, "Advanced Engineering Mathematics", Wiley-India publishers, 10 th edition, 2014. 2. B.V. RAMANA , " Higher engineering mathematics", Tata McGraw-Hill. 3. R.K. Jain and S.R.K. Iyengar, "advanced engineering mathematics", Narosa Publishing House, 5 th edition.		
Course Outcomes: At the end of the course, the student will be able to: CO1: Develop probability distribution of discrete, continuous random variables and joint probability distribution occurring in digital signal processing, information theory and Design engineering. CO2: Understand the analytic functions and application of Bi-linear, Conformal Transformation. CO3: Communications, Know the use of periodic signals and Fourier series to analyse circuits and system. CO4: To use and to apply Fourier Transform, Z-Transform techniques to solve difference equations in Engineering. CO5: Fit a suitable curve by the method of least squares and determine the lines of regression for a set of statistical data		

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	2									2
CO2	3	2									1
CO3	3	3	1								1
CO4	3	2									2
CO5	3	3	1								2

High-3: Medium-2: Low-1

The Evaluation Method

Continuous Internal Evaluation (CIE):

- Three Internal Tests will be conducted for 50 marks each and average of three will be taken. The student should score minimum 30% marks of the average of the three tests to avoid NSSR. **(A)**.
- Alternative Assessment Tools (AAT) are used to complete a project / Quiz/Seminar / Presentation/ other suitable alternate assessment method for 30 marks. Two evaluations will be conducted **(B)**.
- Two Assignments for 10 marks each and the sum of both the assignments will be taken for 20 Marks **(C)**.

Final CIE Marks will be calculated as $(A+B+C)/2$ for 50 marks.

Semester End Examination (SEE):

The question paper consists of two parts, A and B.

Part A: Consists of 10 questions (2 questions from each module) of 2 marks each.

Part B: The question paper should have 10 questions. Each question carries 16 marks. There should be 2 questions from each module, with a maximum of 2 subdivisions. Students must answer any 5 questions choosing one full question from each module.

The SEE Theory marks of 100 will be scaled down to 50.

Final mark for the course is sum of the CIE and SEE Marks.

B.E, III Semester, Electronics Engineering (VLSI Design and Technology)

Computer Organization and Architecture			
Course Code:	MVJ25VL32	Scheme	2025
Type of course	IPCC	Semester	III
Teaching hours / week (L:T:P)	3:0:1	CIE Marks	50
Total Hours of Pedagogy (L:T:P:SL & TW)	42:0:28:50	SEE Marks	50
Credits:	4	Total	100
Examination type (SEE)	Theory	Exam hours	3

Course Objectives:

1. Understand the evolution of computer systems, CPU organization, data representation, instruction formats, and addressing modes used in modern computer architectures.
2. Analyse and implement arithmetic operations using fixed-point arithmetic algorithms, arithmetic logic units (ALUs), and pipelined processing techniques.
3. Explain the design and operation of CPU control units, including hardwired and microprogrammed control, instruction pipelining, superscalar processing, and nano programming.
4. Understand the organization and hierarchy of memory systems, including RAM, cache memory, virtual memory, associative memory, and memory management techniques.
5. Analyse computer communication mechanisms, I/O organization, bus architectures, interrupts, DMA, multiprocessor systems, and compare RISC, CISC, superscalar, and vector processors.

Syllabus

This course provides a comprehensive understanding of Computer Organization and Architecture, covering the evolution and organization of computer systems, data representation, instruction formats, and addressing modes. It introduces arithmetic and logic unit design, including fixed-point operations, multiplication and division algorithms, and pipelined processing. The course also explores CPU control units, hardwired and microprogrammed control, instruction pipelines, and superscalar processing. It covers various memory systems, including RAM, cache, virtual memory, and associative memory. Finally, students gain knowledge of computer communication, buses, I/O organization, interrupts, DMA, multiprocessors, and modern processor architectures such as RISC, CISC, vector, and superscalar processors.

Course Plan**Module I****Fundamentals of Computer Organization and Instruction Processing**

Sr. No	Topics to be covered	Hours required
1	Evolution of Computers: The Mechanical Era, Electronic computers and the later generations. VLSI Era: Integrated circuits, Processor architecture and System architecture	8
2	System Design: System representation, Design process, and the Gate level. Register Level: Register level components, programmable logic devices Processor Level: Processor level components, processor level design	
3	CPU Organization and Data Representation: Fixed-Point Numbers, Floating Point Numbers	
4	Instruction Formats, Instruction Types. Addressing modes.	
Module II		
Computer Arithmetic and Arithmetic Logic Units		
Sr. No	Topics to be covered	Hours required
1	Fixed Point Arithmetic: Addition, Subtraction, Multiplication and division	9
2	Combinational and Sequential ALUs: Carry look ahead adder	
3	Booth’s algorithm, Modified booth’s algorithm and non-restoring division algorithm	
4	Pipeline Processing	
Module III		
CPU Control Unit and Pipeline Processing		
Sr. No	Topics to be covered	Hours required
1	Control design and hardwired control designs.	8
2	Micro programmed Control: multiplier control unit and CPU control unit	
3	Pipeline Control: Instruction pipelines, pipeline performance and superscalar processing.	
4	Nano Programming	
Module IV		
Memory Organization and Hierarchy		
Sr. No	Topics to be covered	Hours required
1	Random Access Memories and Serial - Access Memories	8
2	RAM Interfaces: Magnetic Surface Recording	
3	Memory systems: Multilevel memories, Memory Allocation and Optical Memories	

4	Cache& Virtual Memory, , Associative Memory	
Module V		
Input/Output Organization and Advanced Processor Architectures		
Sr. No	Topics to be covered	Hours required
1	Communication methods: Buses, Bus Control, Bus Interfacing and Bus arbitration	9
2	IO and system control, IO interface circuits, Handshaking, vectored interrupts, PCI interrupts, pipeline interrupts,	
3	IOP organization, DMA and interrupts	
4	Multiprocessors, RISC and CISC processors, Superscalar and vector processor	
Laboratory Experiments		28
1. Write a MATLAB code for the Algorithmic Simulation of Unsigned Binary Addition and Subtraction. 2. Write a MATLAB code for Fixed-Point Data Representation, Arithmetic, and Precision Analysis. 3. Write a MATLAB code for the Implementation of the IEEE 754 Standard Single-Precision Floating-Point Converter. 4. Write a MATLAB code for the Simulation of Binary Multiplication using the Unsigned Partial Product Method. 5. Write a MATLAB code for the Simulation of Instruction Format Parsing and Addressing Mode Selection. 6. Write a MATLAB code for the Algorithmic Simulation of an 8-Bit Arithmetic Logic Unit (ALU). 7. Write a MATLAB code for the Implementation and Simulation of Booth's Multiplication Algorithm. 8. Write a MATLAB code for the Simulation of Binary Division using the Restoring Division Method. 9. Write a MATLAB code for the Simulation and Performance Analysis of Direct-Mapped Cache Memory. 10. Write a MATLAB code for the Algorithmic Simulation of the CPU Fetch-Decode-Execute Cycle.		
Textbooks: 1. John P. Hayes, "Computer architecture and Organisation", Tata McGraw-Hill, 3 rd edition, 2012.		

2. V.Carl Hamacher, Zvonko G.Varanesic and Safat G.Zaky, “Computer Organisation”, Tata McGraw-Hill, 5th edition, 2012.

Reference Books:

1. Morris Mano, “Computer System Architecture”, 3rd edition, Prentice-Hall of India, 2000.
2. Paraami, “Computer Architecture”, Oxford Press, 8th edition, 2011.
3. P.Pal Chaudhuri, “Computer organization and design”, Prentice Hall of India, 2nd edition, 2007.

Other References:

Swayam, NPTEL etc...

Course Outcomes:

The student will be able to:

CO1: To have a thorough understanding of the basic structure and operation of a digital computer

CO2: To discuss in detail the operation of the arithmetic unit including the algorithms & implementation of fixed-point and floating-point addition, subtraction, multiplication & division.

CO3: To study in detail the different types of control and the concept of pipelining.

CO4: To study the hierarchical memory system including cache memories and virtual memory.

CO5: To study the different ways of communicating with I/O devices and standard I/O interfaces.

CO-PO Mapping:

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO 1	PSO 2
CO1	3	3	-	-	-	-	-	-	-	-	-	1	1
CO2	3	3	3	-	-	-	-	-	-	-	-	1	1
CO3	3	3	3	-	-	-	-	-	-	-	-	1	1
CO4	3	3	3	-	-	-	-	-	-	-	-	1	1
CO5	3	3	-	-	-	-	-	-	-	-	-	1	1

High-3: Medium-2: Low-1:

Evaluation Method:

Continuous Internal Evaluation (CIE):

- Three Internal Tests will be conducted for 50 marks each and average of three will be taken. The student should score minimum 30% marks of the average of the three tests to avoid NSSR. **(A)**.
- Alternative Assessment Tools (AAT) are used to complete a project / Quiz/ Seminar cum Presentation / other suitable alternate assessment methods for 30 marks. Two evaluations will be conducted **(B)**.

Final CIE Marks of practical should be calculated as C+D for 50 marks

For IPCC, Final CIE Marks will be calculated as Sum of Theory CIE and Practical CIE for 100 marks.

Semester End Examination (SEE) for Theory:

The question paper consists of two parts, A and B.

Part A: Consists of 10 questions (2 questions from each module) of 2 marks each.

Part B: The question paper should have 10 questions. Each question carries 16 marks. There should be 2 questions from each module, with a maximum of 2 subdivisions. Students have to answer any 5 questions choosing one full question from each module.

The SEE Theory marks of 100 will be scaled down to 50 (X).

Semester End Examination (SEE) for Practical:

The SEE of practical is evaluated for 50 marks, distributed as follows:

Experiment Conduction with Results: 40 marks

Viva Voce: 10 marks

Total 50 marks (Y)

The Final mark for the SEE is X+Y of total 100 marks

Final mark for the course is the sum of CIE and SEE marks, scaled to 100.

- Two Assignments for 10 marks each and the sum of both the assignments will be taken for 20 Marks **(C)**.

Final CIE Marks will be calculated as $(A+B+ C)/2$ for 50 marks:

Continuous Internal Evaluation (CIE) for Practical:

- **Weekly Evaluation for 30 Marks:** Weekly evaluation should be conducted for every experiment. Marks of each evaluation includes Preparedness / Observation (6 Marks) + Experiment Conduction/ Execution (9 Marks) + Viva Voce (9 Marks) + Record Book (6 Marks) for each experiment. All weekly marks are added and scaled to 30 marks **(C)**.
- Two CIE tests for 20 Marks each should be conducted and averaged to 20 Marks. The student should score minimum 30% in the average test marks (i.e. 6 marks) to avoid NSSR. **(D)**.

Final mark for the course is sum of the CIE and SEE Marks:

Course delivery methods		Assessment methods	
1	Chalk and Talk	1	IA tests
2	PPT and Videos	2	Open Book Assignments (OBA)/ Lab Project
3	Flipped Classes	3	Lab Test
4	Practice session/Demonstrations in Labs	4	Semester End Examination
5	Virtual Labs (if present)		

B.E, III Semester, Electronics Engineering (VLSI Design and Technology)

Semester: III			
Analog Electronics			
Course Code	MVJ25VL33	Scheme	2025
Type of course	PCC	Semester	III
Teaching hours / week (L: T:P)	4:0:0:0	CIE Marks	50
Total Hours of Pedagogy (L: T:P:SL & TW)	56:0:0:64	SEE Marks	50
Credits	4	Total	100
Examination type (SEE)	Theory	Exam hours	3
Course Objectives: This course aims to: ● Understand MOS capacitor fundamentals, MOSFET operation, I–V equations, internal capacitances, non-ideal second-order effects, and advanced MOSFET structures. ● Analyze single-stage MOSFET amplifier configurations using small-signal and high-frequency models, and evaluate its gain, terminal resistances, and frequency response. ● Study oscillator circuits and the classification, operational principles, power dissipation, and power conversion efficiency of Class A, B, AB, and C power amplifiers. ● Study capacitor-coupled AC op-amp configurations, methods for setting upper cut-off frequencies. ● Study data converters and active filters and understand the applications of the 555 timer in monostable and astable multivibrator circuits.			
Syllabus			
This course covers MOS capacitor fundamentals (energy band diagram, threshold voltage, C-V characteristics), enhancement/depletion MOSFET device structures, operation, I-V equations, internal capacitances, second-order effects, and advanced FinFET and GAAFET structures. It includes MOSFET small-signal and high-frequency models, common-source, common-gate, and common-drain amplifiers with voltage gain, input/output resistance analysis, and frequency response. The curriculum details OPAMP Wien bridge oscillators, FET-based LC and crystal oscillators, alongside classification, transfer characteristics, power dissipation, and efficiency of Class A, Class B, Class AB, and Class C tuned power amplifiers. The course also covers capacitor-coupled AC op-Amp configurations (inverting, non-inverting, voltage follower, difference amplifiers), setting upper cut-off frequency, instrumentation amplifiers, precision rectifiers, and inverting Schmitt triggers. Finally, it includes weighted-resistor and R-2R ladder DACs, successive-approximation ADCs, first- and second-order low-pass and high-pass filters, band-pass and band-reject filters, 555 timer block diagram, and monostable/astable multivibrators.			
Course Plan			
Module I			
MOSFET Fundamentals			
Sr.	Topics to be covered		Hours

No		required
1	MOS Capacitors: Energy Band Diagram, Threshold Voltage and CV characteristics	11
2	MOSFETs: Enhancement mode MOSFET and Depletion mode MOSFET. Device Structure, Operation, I-V characteristics, I-V equation of MOSFETs.	
3	Second Order Effects in MOSFET: Channel length modulation, Body effect and Subthreshold conduction	
4	MOSFET internal capacitances	
5	Introduction to FinFET and GaaFET	
Module II		
MOSFET Amplifiers		
Sr. No	Topics to be covered	Hours required
1	MOSFET as an Amplifier, Small signal and High frequency models for MOSFETs	12
2	Common-source amplifier: Circuit diagram and small signal analysis, Voltage gain, Input resistance and Output resistance	
3	Common-gate amplifier: Circuit diagram and small signal analysis, Voltage gain, Input resistance and Output resistance	
4	Common-drain amplifier: Circuit diagram and small signal analysis, Voltage gain, Input resistance and Output resistance	
5	Frequency response of MOSFET amplifiers	
Module III		
Oscillators and Power Amplifiers		
1	Oscillators: Wien bridge oscillator using OPAMP, LC and crystal oscillators using FET	11
3	Power amplifiers: Classification of power amplifiers.	
4	Class A power amplifier, Class B power amplifier, power conversion efficiency, power dissipation	
5	Class AB power amplifier and Class C tuned amplifier	
Module IV		
AC Operational Amplifiers and Applications		
Sr. No	Topics to be covered	Hours required
1	Op-Amps as AC Amplifiers: Capacitor coupled inverting amplifier, Capacitor coupled non inverting amplifiers, Setting the upper cut-off frequency	

2	Capacitor coupled voltage follower, Capacitor coupled difference amplifier	11
3	OP-Amp Applications: Instrumentation amplifier, Precision rectifiers, Inverting Schmitt Trigger	

Module V

Data Converters, Filters, and 555 Timer

Sr. No	Topics to be covered	Hours required
1	Digital to Analog Converter : Weighted resistor and R-2R ladder	11
2	Analog to Digital Converter : Successive approximation type	
3	First order and second order Low-pass and high-pass filter	
4	Band- pass and band-reject filters	
5	555 timer: Block diagram, Monostable and astable multivibrators	

Text Books:

1. Robert L. Boylestad and Louis Nashelsky, "Electronic Devices and Circuit Theory", PHI/Pearson Education, 11th edition, 2012.
2. Adel S. Sedra and Kenneth C. Smith, "Microelectronic Circuits", Theory and Applications, Oxford, 6th edition, 2012.
3. Donald A. Neamen "Microelectronics circuit analysis and design", McGraw-Hill Education, 4th edition, 2010.

Reference Books:

1. Behzad Razavi, "Fundamentals of Microelectronics", John Wiley, 2nd edition, 2012.
2. K.A. Navas, "Electronics Lab Manual", Volume I, PHI, 5th edition, 2015.
3. D. Roy Choudhury and Shail B. Jain, "Linear Integrated Circuits", New Age International, 4th edition.

Other References:

1. NPTEL Course: Analog Electronic Circuit, Prof. Shouribrata Chatterjee, IIT Delhi
<https://nptel.ac.in/courses/108102112>
2. Virtual Lab: Analog Electronic Circuit, IIT Kharagpur
<https://aec-iitkgp.vlabs.ac.in/>

Course Outcomes:

At the end of the course, the student will be able to:

CO1: Explain MOS capacitor fundamentals, MOSFET characteristics, second-order effects, and advanced structures.

CO2: Analyze single-stage MOSFET amplifiers, small-signal models, terminal resistances, and frequency response.

CO3: Explain feedback oscillator circuits and evaluate the operating principles, power dissipation, and efficiency of Class A, B, AB, and C power amplifiers.

CO4: Analyze capacitor-coupled AC op-amp configurations, upper cut-off frequency settings, and practical op-amp applications.

CO5: Illustrate the working of DACs, ADCs, active filters, and 555-timer multivibrator circuits.

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	2	1	1			3	2	1	1	
CO2	1				3		1				3
CO3	1	2	3		1		1	2	3		1
CO4	1	2	2	2			1	2	2	2	
CO5	1	1	1		2		1	1	1		2

Evaluation Method

Continuous Internal Evaluation (CIE):

- Three Internal Tests will be conducted for 50 marks each and average of three will be taken. The student should score minimum 30% marks of the average of the three tests to avoid NSSR. **(A)**.
- Alternative Assessment Tools (AAT) are used to complete a project / Quiz/ Seminar cum Presentation / other suitable alternate assessment methods for 30 marks. Two evaluations will be conducted **(B)**.
- Two Assignments for 10 marks each and the sum of both the assignments will be taken for 20 Marks **(C)**.

Final CIE Marks will be calculated as $(A+B+ C)/2$ for 50 marks.

Semester End Examination (SEE):

The question paper consists of two parts, A and B.

Part A: Consists of 10 questions (2 questions from each module) of 2 marks each.

Part B: The question paper should have 10 questions. Each question carries 16 marks. There should be 2 questions from each module, with a maximum of 2 subdivisions. Students have to answer any 5 questions choosing one full question from each module.

The SEE Theory marks of 100 will be scaled down to 50.

High-3: Medium-2: Low-1

Final mark for the course is sum of the CIE and SEE Marks.

Course delivery methods		Assessment methods	
1	Chalk and Talk	1	IA tests
2	PPT and Videos	2	Open Book Assignments (OBA)/ Lab Project
3	Flipped Classes	3	Lab Test
4	Practice session/Demonstrations in Labs	4	Semester Examination End
5	Virtual Labs (if present)		

B.E, III Semester, Electronics Engineering (VLSI Design and Technology)

Network Analysis			
Course Code	MVJ25EC34	Scheme	2025
Type of course	PCC	Semester	III
Teaching hours / week (L: T:P)	3:0:0	CIE Marks	50
Total Hours of Pedagogy (L: T:P:SL & TW)	42:0:0:48	SEE Marks	50
Credits	3	Total	100
Examination type (SEE)	Theory	Exam hours	3
Course Objectives: This course will give ability to: - Describe basic network concepts emphasizing source transformation source shifting, mesh and nodal techniques to solve for resistance/impedance, voltage, current and power. - Explain network Thevenin's, Millman's, Superposition, Reciprocity, Maximum Power transfer and Norton's Theorems and apply them in solving the problems related to Electrical Circuits. - Describe Series and Parallel Combination of Passive Components as resonating circuits, related parameters and to analyze frequency response. - Explain the behavior of networks subjected to transient conditions. Use applications of Laplace transform to solve network problems. - List the two port network parameters like Z, Y, T and h and their inter-relationships.			
Syllabus			
The syllabus covers fundamental electrical network concepts including practical sources, source transformations, and DC circuit analysis using loop and node methods. It introduces graph theory concepts such as trees, matrices, and network equations for systematic analysis. Key network theorems like Superposition, Thevenin's, Norton's, and Maximum Power Transfer are studied for simplifying circuits. Transient behaviour of RL, RC, and RLC circuits is analysed using initial/final conditions and Laplace transforms. Finally, two-port network parameters (Z, Y, h, and transmission) and their interrelationships are explored.			
Course Plan			
Module I			
Sr. No	Topics to be covered		Hours required
1	Basic Concepts: Introduction, Practical sources.		
2	Source transformation.		

3	Star to Delta transformation, Delta to Star transformation.	9
4	Loop and node analysis with linearly dependent and independent sources for DC networks.	
5	Concepts of super node and super mesh.	
Module II		
Sr. No	Topics to be covered	Hours required
1	Graph Theory and Network equations: Graph of a network, Trees, Co-trees and Loops.	8
2	Incidence Matrix.	
3	Tie-set Matrix and loop currents.	
4	Cut-set Matrix.	
5	Analysis of networks, Duality.	
Module III		
Sr. No	Topics to be covered	Hours required
1	Network Theorems: Superposition Theorem.	9
2	Millman's theorem.	
3	Thevenin's theorem and Norton's theorem.	
4	Reciprocity theorem.	
5	Maximum Power transfer theorem (DC networks).	
Module IV		
Sr. No	Topics to be covered	Hours required
1	Transient behaviour and initial conditions: Behaviour of circuit elements under switching condition and their Representation.	8
2	Transient response analysis of series RL Circuits for DC Excitation.	
3	Transient response analysis of series RC Circuits for DC Excitation.	
4	Transient response analysis of series RLC circuit for DC excitations.	
5	Applications of Laplace Transform in circuit Analysis.	
Module V		
Sr. No	Topics to be covered	Hours required
1	Two port network parameters: Introduction, open circuit impedance parameters.	8
2	Short circuit admittance parameters.	
3	Hybrid parameters.	
4	Transmission parameters.	

5	Relationship between parameters, Two port Symmetry and Reciprocity.	
Textbooks:		
1. M.E. Van Valkenberg, "Network analysis", Prentice Hall of India, 3rd edition, 2000. 2. Roy Choudhury, "Networks and systems", New Age International Publications, 2nd edition 2006.		
Reference Books:		
1. Hayt, Kemmerly and Durbin, "Engineering Circuit Analysis", TMH, 7th edition, 2010. 2. J. David Irwin /R. Mark Nelms, "Basic Engineering Circuit Analysis", John Wiley, 8th edition, 2006.		
Other References:(NPTEL/SWAYAM. Any Other)		
1. NPTEL course: Network Analysis, by Prof. Tapas Kumar Bhattacharya, IIT Kharagpur. https://onlinecourses.nptel.ac.in/noc20_ee46		
Course Outcomes:		
At the end of the course, the student will be able to:		
CO1: Determine currents and voltages in a circuit using network simplification techniques.		
CO2: Solve the network problems using graphical methods.		
CO3: Simplify the complex circuits using network theorems.		
CO4: Analyse simple DC circuits and apply the concepts to transient conditions.		
CO5: Solve the given network using specified two port network parameters like Z or Y or T or h and Evaluate frequency response related parameters through the RLC elements, in resonant circuits.		

CO-PO Mapping

CO/PO	PO 1	PO 2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO 11	PS O1	PS O2
CO1	3	3	3	2	2	1					1	2	1
CO2	3	3	3	2	2	1					1	2	2
CO3	3	3	3	2	2	1					1	3	1
CO4	3	3	3	2	2	1					1	3	1
CO5	3	3	3	2	2	1					1	3	2

High-3: Medium-2: Low-1

Evaluation Method

Continuous Internal Evaluation (CIE):

- Three Internal Tests will be conducted for 50 marks each and average of three will be taken. The student should score minimum 30% marks of the average of the three tests to avoid NSSR. **(A)**.
- Alternative Assessment Tools (AAT) are used to complete a project / Quiz/ Seminar cum Presentation / other suitable alternate assessment methods for 30 marks. Two evaluations will be conducted **(B)**.
- Two Assignments for 10 marks each and the sum of both the assignments will be taken for 20 Marks **(C)**.

Final CIE Marks will be calculated as $(A+B+ C)/2$ for 50 marks.

Semester End Examination (SEE):

The question paper consists of two parts, A and B.

Part A: Consists of 10 questions (2 questions from each module) of 2 marks each.

Part B: The question paper should have 10 questions. Each question carries 16 marks. There should be 2 questions from each module, with a maximum of 2 subdivisions. Students have to answer any 5 questions choosing one full question from each module.

The SEE Theory marks of 100 will be scaled down to 50.

The Final mark for the course is sum of the CIE and SEE Marks.

Course delivery methods		Assessment methods	
1	Chalk and talk	1	IA tests
2	PPT and Videos	2	Open Book Assignments (OBA)/ Lab Project
3	Flipped Classes	3	Lab Test
4	Practice session/Demonstrations in Labs	4	Semester End Examination
5	Virtual Labs (if present)		

B.E, III Semester, Electronics Engineering (VLSI Design and Technology)

Analysis and Design of Digital Circuits			
Course Code	MVJ25VL35	Scheme	2025
Type of course	PCC	Semester	III
Teaching hours / week (L: T:P)	3:0:0	CIE Marks	50
Total Hours of Pedagogy (L: T:P:SL & TW)	42:0:0:48	SEE Marks	50
Credits	3	Total	100
Examination type (SEE)	Theory	Exam hours	3

Course Objectives:

This course will give ability to:

- Explain the basic principles of digital logic design, including the operation of logic gates, flip-flops, and the distinction between combinational and sequential circuits.
- Interpret Boolean expressions and demonstrate the use of truth tables and Karnaugh maps in simplifying logical expressions for combinational circuits.
- Apply digital design principles to construct basic combinational circuits.
- Design sequential circuits, such as counters and shift registers, by utilizing flip-flops.
- Design digital systems using programmable logic devices (PLDs).

Syllabus

The course provides a comprehensive understanding of digital logic design, covering the fundamentals of combinational and sequential circuits, including logic simplification, adders, multiplexers, flip-flops, registers, counters, and finite-state machines. It also introduces error-correcting codes, memory devices, and programmable logic devices such as PLA, PAL, and FPGA, enabling students to understand the design and implementation of modern digital systems.

Course Plan**Module I****Principles of Combinational Logic**

Sr. No	Topics to be covered	Hours required
1	Introduction to Combinational logic	8
2	Boolean algebra, SOP/POS forms, Canonical forms.	
3	Generation of switching equations from truth tables, Karnaugh maps- 3, 4 variables	
4	Incompletely specified functions (Don't care terms)	

Module II**Combinational Logic**

Sr.	Topics to be covered	Hours
-----	----------------------	-------

No		required
1	Half adder, Half subtractor and Full adder, subtractor	8
2	Types of adders: Ripple carry adder Look ahead carry adder, parallel adder and subtractor.	
3	BCD adder, binary comparators	
4	Multiplexers and demultiplexers, function realization using MUX	
5	Decoders, encoders, priority encoder, code converters (BCD–Excess-3)	
Module III		
Flip-Flops and its Applications		
Sr. No	Topics to be covered	Hours required
1	Latches and flip-flops (SR, D, T, JK — edge vs level triggered)	9
2	Master-slave JK flip-flop, race-around condition	
3	Flip-flop conversions	
4	Timing hazards, shift registers (SISO/SIPO/PISO/PIPO)	
5	Universal shift register	
6	Counters – synchronous & asynchronous, ripple counters	
Module IV		
Sequential Circuit Design		
Sr. No	Topics to be covered	Hours required
1	Characteristic equations of flip-flops	9
2	Design of sync Mod-N counter (JK/D/T/SR)	
3	Mealy & Moore models, state diagrams/tables	
4	State reduction & state assignment	
5	Design of sequence detector	
6	Error correcting codes (Hamming code)	
Module V		
Memory Devices		
Sr. No	Topics to be covered	Hours required
1	ROM family (ROM, PROM, EPROM, EEPROM), Flash memory	8
2	RAM – static & dynamic, memory expansion	
3	Programmable Logic Devices: Programmable Logic Array (PLA), Programmable Array Logic (PAL)	
4	FPGA architecture (LUTs, CLBs)	

5	Content Addressable Memory (CAM)	
Textbooks:		
1. Morris Mano, "Digital Design," Prentice Hall of India, 3 rd Edition.		
Reference Books:		
1. Charles H Roth Jr. and Larry L. Kinney, "Fundamentals of Logic Design", 7 th Edition.		
2. Donald D. Givone, "Digital Principles and Design", McGraw Hill, 1 st Edition.		
Other References:		
Ex: NPTEL, SWAYAM...etc		
Course Outcomes:		
At the end of the course, the student will be able to:		
CO1 Simplify and analyze digital circuits by Boolean expressions.		
CO2 Analyze and design combinational circuits.		
CO3 Analyze and design sequential circuits.		
CO4 Design digital systems using FSM.		
CO5 Appreciate the role of memory in digital systems.		

CO-PO Mapping

CO/ PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	3	-	-	-	-	-	-	-	-	-	1	1
CO2	3	3	3	-	-	-	-	-	-	-	-	1	1
CO3	3	3	3	-	-	-	-	-	-	-	-	1	1
CO4	3	3	3	-	-	-	-	-	-	-	-	1	1
CO5	3	3	-	-	-	-	-	-	-	-	-	1	1

High-3: Medium-2: Low-1

Evaluation Method

Continuous Internal Evaluation (CIE):

- Three Internal Tests will be conducted for 50 marks each and average of three will be taken. The student should score minimum 30% marks of the average of the three tests to avoid NSSR. **(A)**.

- Alternative Assessment Tools (AAT) are used to complete a project / Quiz/ Seminar cum Presentation / other suitable alternate assessment methods for 30 marks. Two evaluations will be conducted **(B)**.
- Two Assignments for 10 marks each and the sum of both the assignments will be taken for 20 Marks **(C)**.

Final CIE Marks will be calculated as $(A+B+ C)/2$ for 50 marks.

Semester End Examination (SEE):

The question paper consists of two parts, A and B.

Part A: Consists of 10 questions (2 questions from each module) of 2 marks each.

Part B: The question paper should have 10 questions. Each question carries 16 marks. There should be 2 questions from each module, with a maximum of 2 subdivisions. Students have to answer any 5 questions choosing one full question from each module.

The SEE Theory marks of 100 will be scaled down to 50.

Final mark for the course is sum of the CIE and SEE Marks.

Course delivery methods		Assessment methods	
1	Chalk and Talk	1	IA tests
2	PPT and Videos	2	Open Book Assignments (OBA)/ Lab Project
3	Flipped Classes	3	Lab Test
4	Practice session/Demonstrations in Labs	4	Semester End Examination
5	Virtual Labs (if present)		

B.E, III Semester, Electronics Engineering (VLSI Design and Technology)

Digital Circuit Laboratory			
Course Code	MVJ25VLL36	Scheme	2025
Type of course	PCCL	Semester	III
Teaching hours / week (L: T:P)	0:0:2	CIE Marks	50
Total Hours of Pedagogy (L: T:P:SL & TW)	0:0:28:2	SEE Marks	50
Credits	1	Total	100
Examination type (SEE)	Practical	Exam hours	3

Course Objectives:

This course will give ability to:

- Understand digital logic levels and application of knowledge to further understand digital electronics circuits.
- Analyze the design of various digital electronic circuits.
- Apply the knowledge of digital circuits and systems to efficiently, reliably, and economically to achieve desired results.
- Execute the techniques for modelling and troubleshooting circuits and systems through structural and gate-level networks and breadboard designs.
- Analyze the timing diagrams of digital circuits to understand their temporal behavior.

Sl. No.	Experiments List
1.	To realize half/full adder and half/full subtractor.
2.	To realize parallel adder/subtractor using IC7483
3.	To verify BCD to excess 3-code conversion using 7483.
4.	To convert given binary numbers to Gray code using 7486.
5.	To verify truth table of MUX and DEMUX using 74153 and 74139.
6.	To verify the truth table of one bit and two-bit comparators.
7.	To convert a given octal input to binary output and to verify the LED display using 7447 7- segment decoder.
8.	To verify the truth table of SR and T flipflops.
9.	To verify the truth table of JK and D flipflops.

10.	To design 3-bit synchronous counter using T-flipflop.
11.	To verify the truth table of a 4-bit magnitude comparator using IC 7485.
12.	To verify the truth table of an encoder and priority encoder using suitable ICs.
13.	To verify the truth table of a decoder and study its applications using IC 74138.
14.	To design and verify a 3-bit asynchronous (ripple) counter using JK or T flip-flops.
15.	To design and verify a MOD-10 (decade) counter and study its counting sequence.

Course Outcomes:

At the end of the course, the student will be able to:

CO1: Understand the fundamental concepts and techniques used in digital electronics.

CO2: Identify and describe the functions of various digital components.

CO3: Solve boolean functions using logic gates.

CO4: Describe the truth tables of different combinational & sequential circuits.

CO5: Analyze the performance and behavior of digital circuits.

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	3									1
CO2	3	3									1
CO3	3	3									1
CO4	3	3			2				2	1	1
CO5	3	3	3						2	1	1

High-3: Medium-2: Low-1

Evaluation Method

Continuous Internal Evaluation (CIE):

- Weekly Evaluation for 30 Marks: Weekly evaluation should be conducted for every experiment. Marks of each evaluation includes Preparedness / Observation (6 Marks) + Experiment Conduction/ Execution (9 Marks) +

Viva Voce (9 Marks) + Record Book (6 Marks) for each experiment. All weekly marks are added and scaled to 30 marks **(A)**.

- Two CIE tests for 20 Marks each should be conducted and averaged to 20 Marks. The student should score minimum 30% in the average test marks (i.e. 6 marks) to avoid NSSR. **(B)**.

Final CIE Marks of practical should be calculated as A+B for 50 marks.

The Semester End Examination (SEE):

The SEE of practical is evaluated for 50 marks, distributed as follows:

- Experiment Conduction with Results: 40 marks
- Viva Voce: 10 marks
- Total 50 marks

The Final mark for the course is the sum of CIE and SEE Marks.

Course delivery methods		Assessment methods	
1	Chalk and Talk	1	IA tests
2	PPT and Videos	2	Open Book Assignments (OBA)/ Lab Project
3	Flipped Classes	3	Lab Test
4	Practice session/Demonstrations in Labs	4	Semester Examination End
5	Virtual Labs (if present)		

B.E, Electronics Engineering (VLSI Design and Technology)

Sustainable Engineering and SDGs			
Course Code	MVJ25AECK37	Scheme	2025
Type of Course	AEC	Semester	III
Teaching Hours/Week (L:T:P)	1:0:0	CIE Marks	50
Total Hours of Pedagogy (L:T:P:SL&TW)	14:0:0:16	SEE Marks	50
Credits	1	Total Marks	100
Examination type (SEE)	Theory	Exam Hours	2 Hrs.
Course Objectives: This course will give ability to: • Explain the basic concepts of sustainability, sustainable development and the role of engineers. • Describe the 17 Sustainable Development Goals (SDGs) and relate selected SDGs to engineering disciplines. • Explain basic sustainable-engineering principles including resource efficiency, systems thinking, life cycle thinking and circular economy. • Identify environmental, social and economic impacts associated with engineering products, processes and services. • Apply simple sustainability thinking to propose an improved solution to a real-life engineering problem.			
Syllabus			
Objective of this course is to inculcate in students an awareness of environmental issues and the global initiatives towards attaining sustainability. The student should realize the potential of technology in bringing in sustainable practices.			
Module I			
Sr. No	Topics to be covered		Hours required
1	Foundations of Sustainability and Role of Engineers: Sustainability: Introduction, concept, evolution of the concept; Social, environmental and economic sustainability concepts; Sustainable development, Nexus between Technology and Sustainable development; Millennium Development Goals (MDGs) and Sustainable Development Goals (SDGs)-Overview of the 17 SDGs, Clean Development Mechanism (CDM), Introduction to the UN 2030 Agenda.		3
Module II			
Sr. No	Topics to be covered		Hours required
1	Environmental Pollution: Air Pollution and its effects, Water pollution and its sources, Zero waste concept and 3 R concepts in solid waste management; Greenhouse effect, Global warming, Climate change, Ozone layer depletion, Carbon credits, carbon trading and carbon footprint, legal provisions for environmental protection.		3
Module III			
Sr. No	Topics to be covered		Hours required

1	Environmental management standards: ISO 14001:2015 framework and benefits, Scope and goal of Life Cycle Analysis (LCA), Sustainable Engineering Principles and Circular Economy, Bio-mimicking, Environment Impact Assessment (EIA), Industrial ecology and industrial symbiosis.	3
----------	--	----------

Module IV

Sr. No	Topics to be covered	Hours required
1	Resources and its utilisation: Basic concepts of Conventional and non-conventional energy, Environmental footprints, General idea about solar energy, Fuel cells, Wind energy, Small hydro plants, biofuels, Energy derived from oceans and Geothermal energy.	3

Module V

Sr. No	Topics to be covered	Hours required
1	Sustainable design and practices/Case Studies/Student Activity: Sustainability practices: Basic concept of sustainable habitat, conventional design Vs sustainable design, Methods for increasing energy efficiency in buildings, Green Engineering, Sustainable Urbanisation, Sustainable cities, Sustainable transport.	2

Textbooks:

1. Toolseeram Ramjeawon, Introduction to Sustainability for Engineers, CRC Press, 1st Edition, 2020.
2. Rag, R. L. and Ramesh Lakshmi Dinachandran, Introduction to Sustainable Engineering, PHI Learning.
3. Allen, D. T. and Shonnard, D. R., Sustainability Engineering: Concepts, Design and Case Studies, Prentice Hall.
4. Bradley. A.S; Adebayo,A.O., Maria, P. Engineering applications in sustainable design and development, Cengage learning
5. Ni bin Chang, Systems Analysis for Sustainable Engineering: Theory and Applications, McGraw-Hill Professional.

Reference Books:

1. ECBC Code 2007, Bureau of Energy Efficiency, New Delhi Bureau of Energy Efficiency Publications- Rating System, TERI Publications - GRIHA Rating System
2. Environment Impact Assessment Guidelines, Notification of Government of India, 2006
3. Allenby, B. R., The Sustainability Engineering Handbook, McGraw-Hill.
4. Mihelcic, J. R. and Zimmerman, J. B., Environmental Engineering: Fundamentals, Sustainability, Design, Wiley.
5. Mackenthun, K.M., Basic Concepts in Environmental Management, Lewis Publication, London, 1998
6. Twidell, J. W. and Weir, A. D., Renewable Energy Resources, English Language Book Society (ELBS).
7. Purohit, S. S., Green Technology - An approach for sustainable environment, Agrobios Publication

Course Outcomes:

At the end of the course, the student will be able to:

CO1: Explain sustainability, sustainable development and the role of engineers

CO2: Explain different types of environmental pollution problems, SDGs, relate them to engineering applications, and their sustainable solutions

CO3: Explain life cycle thinking and environmental footprints

CO4: Apply basic principles of sustainable engineering and circular economy

CO5: Propose a basic sustainable engineering solution to a real-life problem

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	1					2	3				
CO2	1				1	2	3				
CO3					1	2	3				
CO4					1	2	3				
CO5						2	3				

High-3: Medium-2: Low-1

Evaluation Method

Continuous Internal Evaluation (CIE) – 50 Marks

The CIE for the mandatory credit courses common across all disciplines comprises of two components as follows:

Internal Assessment Tests (30 Marks):

Two Internal Assessment tests will be conducted, each comprising 50 multiple choice questions for a total of 50 marks. The average of the two test scores will be scaled down to 30 marks.

Assignments (20 Marks):

Students are required to complete two assignments, each carrying 10 marks. These assignments may include projects*, poster presentations*, seminars*, or similar academic activities. The marks of the two assignments are added to get 20 marks.

*Each assignment will undergo two rounds of evaluation to assess progress and quality

At the beginning of the semester, the instructor/faculty teaching the course has to announce the methods of Assignment for the course.

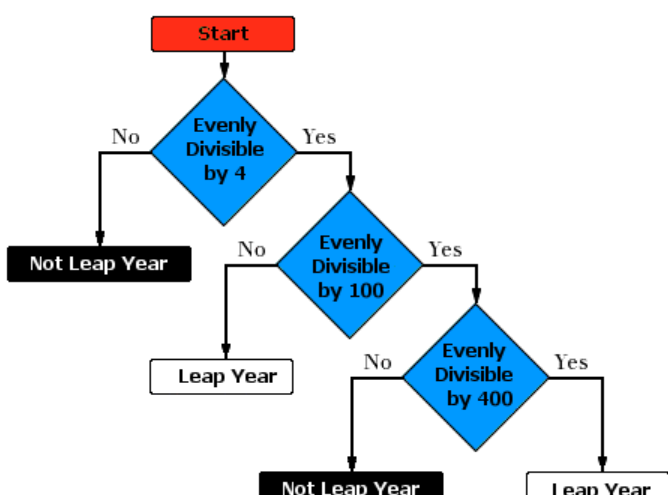
Together, these two components are added to get the Final CIE marks of 50.

Semester End Examination (SEE) – 50 Marks

A Semester End Examination is conducted for 50 marks comprising of multiple-choice questions (MCQ) type each of one mark.

The final score for the course out of 100 is the SumTotal of SEE and CIE.

B.E, Electronics Engineering (VLSI Design and Technology)

LabVIEW for ECE			
Course Code	MVJ25EC38SL	Scheme	2025
Type of Course	SDL	Semester	III
Teaching Hours/Week (L:T:P)	0:0:2	CIE Marks	50
Total Hours of Pedagogy (L:T:P:SL&TW)	0:0:28:2	SEE Marks	50
Credits	1	Total Marks	100
Examination type (SEE)	Practical	Exam Hours	3
Course Objectives: This course will enable students to, • Introduce the basics of LabVIEW environment and the basic concept of Data Flow programming. • Familiarize the common LabVIEW functions with the different palettes. • Understand the graphical programming and the debugging methods. • Understand the advanced operations of LabVIEW programming in developing stand alone applications. • Understand the modularity in different data types and modularity in different operations of LabVIEW.			
Sl. No.	Experiments List		
1.	Build a VI to develop code converters like binary to gray, gray to binary, BCD to Excess 3.		
2.	Build a VI to perform the operation of Half adder and Full adder.		
3.	Build a VI to find whether the given input year is a leap year or not.  <pre> graph TD Start([Start]) --> D1{Evenly Divisible by 4} D1 -- No --> NLY1[Not Leap Year] D1 -- Yes --> D2{Evenly Divisible by 100} D2 -- No --> LY1[Leap Year] D2 -- Yes --> D3{Evenly Divisible by 400} D3 -- No --> NLY2[Not Leap Year] D3 -- Yes --> LY2[Leap Year] </pre>		
4.	Build a VI for Tank level measurement. (Single tank level filling and then draining, Two tank with one filling and other draining after first tank filling, two tanks simultaneously One filling and other draining)		
5.	Build a VI to add 'n' Natural numbers according to the input of the user.(Using feedback node and shift register)		
6.	Build a VI to find the Fibonacci series according to the given input of the user.		
7.	Build a VI to find the factorial of a given number.		
8.	Build a VI to display only the odd numbers and even numbers separately using conditional tunnel modes.		

9.	Build a VI to simulate traffic light control.
Course Outcomes: The student will be able to: CO1: Understand the basic tools for developing the Virtual Instruments environment. CO2: Analyse data structures of different data types of Numeric, Boolean in LabVIEW and Identify and use various loop structures in LabVIEW environment. CO3: Understand the different operational functions for arrays and clusters to develop different tasks. CO4: Examine Digital waveform graphs and Charts and Implement error handling techniques in LabVIEW.	

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	2	2	2		2				2		2
CO2			2	2	2						
CO3			2		2				2		
CO4			2		2				2		
CO5			2		2					2	

High-3: Medium-2: Low-1

Evaluation Method:

Continuous Internal Evaluation (CIE):

The CIE is evaluated for 50 marks, distributed as follows: Regular Laboratory Performance & Conduct (15 Marks) + Module Project Evaluations (3 Projects) (20 Marks) + Laboratory Record / Logbook & Calculations (10 Marks) + Internal Practical Test / Quizzes (5 Marks)

Final CIE Marks of practical should be calculated for 50 marks.

Semester End Examination (SEE):

The question paper consists of two parts, A and B.

Part A: Consists of 10 questions (2 questions from each module) of 2 marks each.

Part B: The question paper should have 10 questions. Each question carries 16 marks.

There should be 2 questions from each module, with a maximum of 2 subdivisions.

Students have to answer any 5 questions choosing one full question from each module.

The SEE Theory marks of 100 will be scaled down to 50.

The Final mark for the course is sum of the CIE and SEE Marks.

B.E, III Semester, Electronics Engineering (VLSI design and Technology)

SEMESTER III		
PHYSICAL EDUCATION (SPORTS & ATHLETICS)		
Course Code:	MVJ25PE39	CIE Marks: 100
L: T:P:S	0:0:0:28	SEE Marks: -
Credits:	0	Total :100
Hours:	28	SEE Duration: -
Course Objectives: the student will be able to		
1	Understand the meaning and importance of the fitness and the benefits of fitness	
2	Types of fitness and fitness tips.	
3	Importance of Sports, and Yoga in a day-to-day life.	
4	Understand the importance of aerobics and other activities for healthy lifestyle.	
5	Know about the different roles of organization and administration in sports events.	
Topics / Activities to be Covered (100Marks)		
Module I		5Hours
Orientation		
➤ Lifestyle		
➤ Fitness		
➤ Food & Nutrition: Sports diet.		
➤ Stress Management		
Module II		5 Hours
General Fitness & Components of Fitness		
➤ Warming up (Free Hand Exercises).		
➤ Strength—Push-up/Pull-ups		
➤ Speed—30MtrDash.		
➤ Agility—Shuttle Run		
➤ Flexibility—Sit and Reach		
Module III		6 Hours
Specific Games (Anyone to be selected by the student)		
➤ Volleyball— Attack, Block, Service, Upper Hand Pass and Lower Hand and Pass.		

➤ Throw ball—Service, Receive, Spin attack, Net Drop & Jump throw. ➤ Kabaddi— Hand touch, Toe Touch, Thigh Hold, Ankle hold and Bonus. ➤ Basketball-dribbling, passing, shooting etc. ➤ Table Tennis—Service (Fore Hand & Back Hand) ➤ Receive (Fore Hand & Back Hand) ➤ Smash, Athletics (Track / Field Events) -Running, Jumping, Throwing.		
Module IV		6 Hours
Role of Organization and administration		
➤ Planning. ➤ Organizing. ➤ Staffing. ➤ Directing. ➤ Coordinating & controlling. ➤ Reporting & Recording. ➤ Budgeting.		
Module V		6Hours
Aerobics		
➤ Dance Aerobics ➤ Sport Aerobics ➤ Warm up Aerobics ➤ Cardiovascular Aerobics		
Course Outcomes: After completing the course, the students will be able to		
CO1	Understand the fundamental concepts and skills of Physical Education, Health, Nutrition and Fitness.	
CO2	Familiarization of health-related Exercises, Sports for overall growth and development.	
CO3	Create a foundation for the professionals in physical Education and Sports.	
CO4	Participate in the competition at regional / state / national / international levels.	
CO5	Create consciousness among the students on Health, Fitness and Wellness in developing and maintaining a healthy lifestyle.	
Assessment Details for CIE (both CIE and SEE)		
Weight age	CIE – 100%	• Implementation strategies

Participation of student in all the modules	50 Marks	of the project (PE work). • The last report should be signed by PED, the HOD and principal. • At last report should be evaluated by the PED of the institute. • Finally, the consolidated marks sheet should be sent to the Controller of Examinations office.
Final presentation / exhibition / Participation In competitions / practical on specific tasks Assigned to the students	50 Marks	
Total marks for the course in eachsemester	100 Marks	
Marks scored for 100 by the students should be Scale to 50 marks in each semester.		
Students should present the progress of the activities as per the schedule in the prescribed practical session in the field. There should be positive progress in the vertical order for the benefit of society in general.		

CO/PO Mapping											
CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11
CO 1	-	-	-	-	-	-	-	2	2	-	-
CO 2	-	-	-	-	-	-	-	2	2	-	-
CO 3	-	-	-	-	-	-	-	2	2	-	-
CO 4	-	-	-	-	-	-	-	2	2	-	-
CO 5	-	-	-	-	-	-	-	3	3	-	-

B.E, Electronics Engineering (VLSI Design and Technology)

YOGA			
Course Code	MVJ25YO39	Scheme	2025
Type of Course	NCMC	Semester	III
Teaching Hours/Week (L: T: P)	0:0:0	CIE Marks	100
Total Hours of Pedagogy (L: T: P: SL&TW)	0:0:0:28	SEE Marks	--
Credits	0	Total Marks	100
Examination type (SEE)	--	Exam Hours	--
Course Learning Objectives: The students will be able to			
1	Promote Holistic Wellness Practice in Students.		
2	Develop Physical Awareness and Flexibility		
3	Improve Focus and Academic Performance		
4	Encourage Healthy Lifestyle Habits.		
5	Support mental Health and Emotional balance.		
<u>The Health Benefits of Yoga:</u>			
1)Yoga helps with a person-centered approach to well-being offering physical, mental(cognitive), and spiritual(emotional) benefits for students. These benefits can help students cope with the demands of academic journeys, improve their overall health, and promote personal development.			
● Key Benefits of Various Yoga Techniques: ● Enhances Physical Well-being. ● Boosts Mental Focus. ● Promotes Emotional Stability. ● Reduce Stress Levels. ● Encourages Inner Growth.			
It is also used as an adjunct therapy to support recovery from various physical health conditions such as:			
● Chronic Pain. ● Back Pain. ● Arthritis. ● Cardiovascular Diseases. ● Asthma. ● Chronic Fatigue Syndrome. ● Menstrual Disorders. ● Digestive Issues. ● Thyroid Imbalances. ● Migraine and headache.			
2) Core observations on how yoga functions as a complementary mind-body intervention to support the psychological, physiological and spiritual healing processes associated with various health conditions.			
Psychological Benefits:			
● Stress reduction. ● Anxiety relief. ● Trauma healing. ● Cognitive and clarity focus. ● Emotional Regulation.			

• Aid in managing depression. Physiological Benefits: • Enhance Blood Circulation. • Boost Cardiovascular Health. • Supports Overall Gut Function. • Promotes Thyroid Function. • Relief from Headaches. • Increased Energy level. Spiritual Benefits: • Cultivating gratitude and Compassion • Self–realization • Balance and Harmony • Inner Peace • Sense of oneness. Mindfulness	
MODULE- I	
Discipline and Awareness Reflect Habits s Thoughts: • Basic theory of Yoga, Yamas s Niyamas Yoga definition, Aims and Objectives, importance of yoga in students. • Introduction to Yoga asana Yoga asana meaning, principle and health benefits. • Ashtanga yoga Meaning, breathing techniques. • Four paths of yoga Karma yoga, Bhakthi yoga, Raja yoga, Jnana yoga. • Surya namaskar Surya namaskar prayer and its meaning, benefits and importance. • Yoga asanas Asanas it's need, importance, name and technique. Sitting: -Vajrasana, - adasana, Ardachakrasana, Prone line: -Advasana, Bhujangasana Supine line: -Shavasana, Supta baddhakonasana, Balancing posture: -Vrikshasana, Garudasana	7 Hrs
MODULE -II	
Building strength and focus Finding out the obstacle: • Kriya Yoga Tapas, Svadhyaya, Ishwarapranidhana • Five Kleshas Obstacles. • Pranayama Introduction to Pranayama. • Pratyahara Preparing mind for meditation, Breathe focus techniques.	7 Hrs

• Yoga asanas Standing: -Virabhadrasana, Parshvakona Sitting: -Vajrasana, Paschimottanasana Prone Line: - Dhanurasana, Shalabhasana, Supine Line: -Ananda Balasana, Supta Matsyendrasana , Balancing: -Natarajasana (Dancer Pose)	
MODULE -III	
Awareness and inner balance: Finding how focused is the mind • Dharana: Concentration • Dhyana: Meditation • Swasthya, Smriti, Sankalpa. Tool of academic excellence. • Samyama Patanjali's concept of samyama • Yogasanas Standing: - ArdhaChandrasana, Utkatasana Sitting: - Padmasana (or prep), Gomukhasana Prone Line: - Adho Mukha Svanasana, Naukasana Supine Line: - SuptaBaddhaKonasana, Chakrasana Balancing: - Garudasana (Eagle Pose)	7 Hrs
MODULE -IV	
Integrating Yoga in daily Life: • Yama niyama Acharam: Practice of ethical Discipline (practicing nonviolence, truth, cleanliness) • Ahara- Vihara Samyama: Practice discipline in diet C lifestyle. • Asana- pranayama sadhana: Daily practice of asanas and pranayama • Yogasanas: Standing: -PrasaritaPadottanasana, ParivrttaTrikonasana Sitting: -Baddha Konasana, Marichyasana Prone Line: -Ustrasana (Camel), Makarasana (relaxation) Supine Line: -Sarvangasana, Shavasana Balancing: - Bakasana (Crow – optional or modified)	7 Hrs

Course outcomes	
CO1	Identify and reflect on personal habits and thoughts.
CO2	Explain the basic theory of Yoga, including Yamas C Niyama.
CO3	Understand the definition, aims, objectives, and importance of Yoga, especially for students.
CO4	Enhance physical and mental strength through advanced Yog asanas.

CO/PO Mapping											
CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11
CO 1		2						3	2	2	
CO 2	2						2	2			
CO 3	2					2	2	3			
CO 4					2		3	3			

Weekley assessment will be done by the instructor by giving different poses / Asanas.

The final assessment scaled up to 100 marks.

Text Book

1	Ajitkumar, "Yogapravesha in Kannada"
2	BKS Iyengar "Light on Yoga"

Reference Books

1	M L Gharote & Dr. S K Ganguly, "Teaching Methods for Yogic practices"
2	Yoga Instructor Course hand book published by SVYASA University, Bengaluru
3	Yamini Muthanna," Yoga for Children –step by step"

B.E, Electronics Engineering (VLSI Design and Technology)**Additional Mathematics-I**

Course Code	MVJ25MATDIP310	Scheme	2025
Type of Course	NCMC	Semester	III
Teaching Hours/Week (L: T: P)	2:0:0	CIE Marks	100
Total Hours of Pedagogy (L: T: P: SL&TW)	28:0:0:0	SEE Marks	--
Credits	0	Total Marks	100
Examination type (SEE)	--	Exam Hours	--

Course Objectives:

This course will give ability to:

- To familiarize the important and introductory concepts of Differential calculus, Integral calculus, Vector differentiation, Probability, ordinary differential equations of first order, and analyze the engineering problems.

Syllabus

Differential calculus-nth derivative, Leibnitz theorem, Polar curves - angle between the radius vector and tangent, angle between two curves pedal equation, Taylor's and Maclaurin's series expansions, Integral Calculus: Statement of reduction formulae for the integrals of $\sin^n(x)$, $\cos^n(x)$, $\sin^n x$, $\cos^m x$, Evaluation of these integrals with standard limits-problems, Double -Simple examples, Triple integrals, Vector Differentiation: Differentiation of vector functions, Velocity and acceleration of a particle moving on a space curve, Scalar and Vector point functions, Gradient, Divergence, Curl, Solenoidal and Irrotational vector fields, Vector identities - $\text{div}(\phi \vec{A})$, $\text{curl}(\phi \vec{A})$, $\text{curl}(\text{grad}(\phi))$, $\text{div}(\text{curl} \vec{A})$, Probability: Basic terminology, Sample space and events, Axioms of probability. Addition and multiplication theorems, Conditional probability, Bayes theorem, Introduction – Formation of differential equation, solutions of first order and first-degree differential equations, Variable separable form, homogeneous Exact, linear differential equations, Clairaut's equation.

Course Plan**Module I****Differential calculus**

Sr.No	Topics to be covered	Hours required
1	Differential calculus: Recapitulation of successive differentiation -nth derivative	6
2	Leibnitz theorem (without proof) and Problems	
3	Polar curves - angle between the radius vector and tangent, angle between two curves	
4	pedal equation	
5	Taylor's and Maclaurin's series expansions- Illustrative examples	

Module II**Integral Calculus**

Sr. No	Topics to be covered	Hours required
1	Integral Calculus: Statement of reduction formulae for the integrals of $\sin^n(x)$, $\cos^n(x)$, $\sin^n x$, $\cos^m x$	6
2	Evaluation of these integrals with standard limits-problems	
3	Double -Simple examples	

4	Triple integrals-Simple examples	
Module III		
Vector Differentiation		
Sr. No	Topics to be covered	Hours required
1	Vector Differentiation: Differentiation of vector functions	6
2	Velocity and acceleration of a particle moving on a space curve	
3	Scalar and Vector point functions, Gradient, Divergence, Curl	
4	Solenoidal and Irrotational vector fields	
5	Vector identities - $\text{div}(\phi \vec{A})$, $\text{curl}(\phi \vec{A})$, $\text{curl}(\text{grad}(\phi))$, $\text{div}(\text{curl} \vec{A})$.	
Module IV		
Probability		
Sr. No	Topics to be covered	Hours required
1	Probability: Basic terminology, Sample space and events	5
2	Axioms of probability. Addition and multiplication theorems	
3	Conditional probability – illustrative examples	
4	Bayes theorem-examples	
Module V		
Ordinary Differential Equations of First Order		
Sr. No	Topics to be covered	Hours required
1	Introduction – Formation of differential equation, solutions of first order and first degree differential equations	5
2	Variable separable form, homogeneous	
3	Exact, linear differential equations	
4	Some special first order equations: Clairaut’s equation	
5	Some special first order equations: Clairaut’s equation	
Textbooks:		
1. B.S. Grewal, “Higher Engineering Mathematics” Khanna Publishers, 43rd Edition, 2013. 2. Ramana B. V., “Higher Engineering Mathematics”, Tata Mc Graw-Hill, 2006.		
Reference Books:		
3. Erwin Kreyszig, “Advanced Engineering Mathematics”, Wiley-India publishers, 10th edition, 2014. 4. G. B. Gururajachar: Calculus and Linear Algebra, Academic Excellent Series Publication, 2018-19		
Other References:(NPTEL/SWAYAM. Any Other)		
1. https://youtube.com/playlist?list=PL7oBzLzHZ1wXBSiJEgqz_iwVoLiY8qhbv&si=LWY0G3yww0MbHN9G NPTEL course: Mechanics of Materials by Dr. U Saravanan, IIT Madras 1. https://youtu.be/rveuCHNkaC4?si=jIJomstkFZySE0tk Mechanics of Solids by Prof. Priyanka Ghosh, IIT Kanpur. 2. https://youtu.be/U-5tA9ZMsno?si=Wcl7W7JN3Wmg3McP 3. https://youtu.be/COI0BUmNHT8?si=77D82b9BAnf-jVT2 4. https://youtu.be/ES741wq3APA?si=iqR2QZ5xreoVGo1v		

Course Outcomes:

At the end of the course, the student will be able to:

- CO1:** Apply the knowledge of calculus to solve problems related to polar curves and its applications
- CO2:** Apply the concept of integration and variables to evaluate multiple integrals and their usage in computing the area and volumes.
- CO3:** Illustrate the applications of multivariate calculus to understand the solenoidal and irrotational vectors and also exhibit the inter dependence of line, surface and volume integrals.
- CO4:** Understand the basic Concepts of Probability
- CO5:** Recognize and solve first-order ordinary differential equations occurring in different branches of engineering

CO-PO Mapping:

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	3		2						1	1
CO2	3	3		2						1	1
CO3	3	3		3							1
CO4	2	2		3						1	1
CO5	2	2		2							1

High-3: Medium-2: Low-1:

Evaluation Method:**Continuous Internal Evaluation (CIE):**

- Two CIE Will be conducted for 50 marks each and average of two will be taken (A)
- Alternative Assessment Tools (AAT) should be a project / Quiz/ Seminar cum Presentation / other suitable alternate assessment methods for 30 marks. Two evaluations will be conducted (B)
- Two Assignments for 10 marks each and the sum of both the assignments will be taken for 20 Marks (C)

Final CIE Marks will be calculated as (A+B+C) for 100 marks

Course delivery methods		Assessment methods	
1	Chalk and talk	1	IA tests
2	PPT and Videos	2	Open Book Assignments (OBA)/ Lab Project
3	Flipped Classes	3	AAT (Quiz, Mini Project)